PIC12F683
Data Sheet

8-Pin Flash-Based, 8-Bit CMOS Microcontrollers with nanoWatt Technology
Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KeeLog, KeeLog logo, microD, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries. AmpLab, FilterLab, Linear Active Thermistor, Migratable Memory, MXDEV, MXLAB, PS logo, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICWorks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSIP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rLab, rPICDEM, Select Mode, Smart Serial, SmartTel, Total Endurance, UNI/O, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2007, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon; and Mountain View, California. The Company’s quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOG® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001:2000 certified.
8-Pin Flash-Based, 8-Bit CMOS Microcontrollers with nanoWatt Technology

High-Performance RISC CPU:
- Only 35 instructions to learn:
  - All single-cycle instructions except branches
- Operating speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:
- Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency range of 8 MHz to 125 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - Crystal fail detect for critical applications
  - Clock mode switching during operation for power savings
- Power-Saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and Extended temperature range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection
- High Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM Retention: > 40 years

Low-Power Features:
- Standby Current:
  - 50 nA @ 2.0V, typical
- Operating Current:
  - 11 μA @ 32 kHz, 2.0V, typical
  - 220 μA @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical

Peripheral Features:
- 6 I/O pins with individual direction control:
  - High current source/sink for direct LED drive
  - Interrupt-on-pin change
  - Individually programmable weak pull-ups
  - Ultra Low-Power Wake-up on GP0
- Analog Comparator module with:
  - One analog comparator
  - Programmable on-chip voltage reference (CVREF) module (% of VDD)
  - Comparator inputs and output externally accessible
- A/D Converter:
  - 10-bit resolution and 4 channels
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Timer1 Gate (count enable)
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture, Compare, PWM module:
  - 16-bit Capture, max resolution 12.5 ns
  - Compare, max resolution 200 ns
  - 10-bit PWM, max frequency 20 kHz
- In-Circuit Serial Programming™ (ICSP™) via two pins

Device | Program Memory | Data Memory | I/O | 10-bit A/D (ch) | Comparators | Timers 8/16-bit
--- | --- | --- | --- | --- | --- | ---
PIC12F683 | 2048 | 128 | 256 | 6 | 4 | 1 | 2/1

© 2007 Microchip Technology Inc.
TABLE 1: 8-PIN SUMMARY

<table>
<thead>
<tr>
<th>I/O</th>
<th>Pin</th>
<th>Analog</th>
<th>Comparators</th>
<th>Timer</th>
<th>CCP</th>
<th>Interrupts</th>
<th>Pull-ups</th>
<th>Basic</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP0</td>
<td>7</td>
<td>AN0</td>
<td>CIN+</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOC</td>
<td>Y</td>
</tr>
<tr>
<td>GP1</td>
<td>6</td>
<td>AN1/VREF</td>
<td>CIN-</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOC</td>
<td>Y</td>
</tr>
<tr>
<td>GP2</td>
<td>5</td>
<td>AN2</td>
<td>COUT</td>
<td>T0CKI</td>
<td>CCP1</td>
<td>INT/IOC</td>
<td>Y</td>
<td>—</td>
</tr>
<tr>
<td>GP3(1)</td>
<td>4</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOC</td>
<td>Y(2)</td>
<td>MCLR/VPP</td>
</tr>
<tr>
<td>GP4</td>
<td>3</td>
<td>AN3</td>
<td>—</td>
<td>T1G</td>
<td>—</td>
<td>—</td>
<td>IOC</td>
<td>Y</td>
</tr>
<tr>
<td>GP5</td>
<td>2</td>
<td>—</td>
<td>T1CKI</td>
<td>—</td>
<td>IOC</td>
<td>Y</td>
<td>Y</td>
<td>OSC1/CLKIN</td>
</tr>
<tr>
<td>—</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>—</td>
<td>8</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Note 1: Input only.
Note 2: Only when pin is configured for external MCLR.
# Table of Contents

1.0 Device Overview .................................................................................................................. 5  
2.0 Memory Organization .......................................................................................................... 7  
3.0 Oscillator Module (With Fail-Safe Clock Monitor) ............................................................... 19  
4.0 GPIO Port .......................................................................................................................... 31  
5.0 Timer0 Module ................................................................................................................ 41  
6.0 Timer1 Module with Gate Control ..................................................................................... 44  
7.0 Timer2 Module ................................................................................................................ 49  
8.0 Comparator Module ......................................................................................................... 51  
9.0 Analog-to-Digital Converter (ADC) Module ...................................................................... 61  
10.0 Data EEPROM Memory .................................................................................................... 71  
11.0 Capture/Compare/PWM (CCP) Module .......................................................................... 75  
12.0 Special Features of the CPU .......................................................................................... 83  
13.0 Instruction Set Summary .................................................................................................. 101  
14.0 Development Support .................................................................................................... 111  
15.0 Electrical Specifications .................................................................................................. 115  
16.0 DC and AC Characteristics Graphs and Tables ............................................................... 137  
17.0 Packaging Information .................................................................................................... 159  
Appendix A: Data Sheet Revision History ............................................................................ 165  
Appendix B: Migrating From Other PIC® Devices ................................................................. 165  
The Microchip Web Site .......................................................................................................... 171  
Customer Change Notification Service .................................................................................. 171  
Customer Support ................................................................................................................ 171  
Reader Response ................................................................................................................ 172  
Product Identification System ............................................................................................... 173  

---

## TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at docerrors@microchip.com or fax the Reader Response Form in the back of this data sheet to (480) 792-4150. We welcome your feedback.

### Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip’s Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

### Customer Notification System

Register on our web site at [www.microchip.com](http://www.microchip.com) to receive the most current information on all of our products.
1.0 DEVICE OVERVIEW

The PIC12F683 is covered by this data sheet. It is available in 8-pin PDIP, SOIC and DFN-S packages. Figure 1-1 shows a block diagram of the PIC12F683 device. Table 1-1 shows the pinout description.
## TABLE 1-1: PIC12F683 PINOUT DESCRIPTION

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Input Type</th>
<th>Output Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>Vdd</td>
<td>Power</td>
<td>—</td>
<td>Positive supply</td>
</tr>
<tr>
<td>GP5/T1CKI/OSC1/CLKIN</td>
<td>GP5</td>
<td>TTL</td>
<td>CMOS</td>
<td>GPIO I/O with prog. pull-up and interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>T1CKI</td>
<td>ST</td>
<td>—</td>
<td>Timer1 clock</td>
</tr>
<tr>
<td></td>
<td>OSC1</td>
<td>XTAL</td>
<td>—</td>
<td>Crystal/Resonator</td>
</tr>
<tr>
<td></td>
<td>CLKN1</td>
<td>ST</td>
<td>—</td>
<td>External clock input/RC oscillator connection</td>
</tr>
<tr>
<td>GP4/AN3/T1G/OSC2/CLKOUT</td>
<td>GP4</td>
<td>TTL</td>
<td>CMOS</td>
<td>GPIO I/O with prog. pull-up and interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>AN3</td>
<td>AN</td>
<td>—</td>
<td>A/D Channel 3 input</td>
</tr>
<tr>
<td></td>
<td>T1G</td>
<td>ST</td>
<td>—</td>
<td>Timer1 gate</td>
</tr>
<tr>
<td></td>
<td>OSC2</td>
<td>XTAL</td>
<td>—</td>
<td>Crystal/Resonator</td>
</tr>
<tr>
<td></td>
<td>CLKOUT</td>
<td>—</td>
<td>CMOS</td>
<td>Fosc/4 output</td>
</tr>
<tr>
<td>GP3/MCLR/VPP</td>
<td>GP3</td>
<td>TTL</td>
<td>—</td>
<td>GPIO input with interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>MCLR</td>
<td>ST</td>
<td>—</td>
<td>Master Clear with internal pull-up</td>
</tr>
<tr>
<td></td>
<td>VPP</td>
<td>HV</td>
<td>—</td>
<td>Programming voltage</td>
</tr>
<tr>
<td>GP2/AN2/T0CKI/INT/COUT/CCP1</td>
<td>GP2</td>
<td>ST</td>
<td>CMOS</td>
<td>GPIO I/O with prog. pull-up and interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>AN2</td>
<td>AN</td>
<td>—</td>
<td>A/D Channel 2 input</td>
</tr>
<tr>
<td></td>
<td>T0CKI</td>
<td>ST</td>
<td>—</td>
<td>Timer0 clock input</td>
</tr>
<tr>
<td></td>
<td>INT</td>
<td>ST</td>
<td>—</td>
<td>External Interrupt</td>
</tr>
<tr>
<td></td>
<td>COUT</td>
<td>—</td>
<td>CMOS</td>
<td>Comparator 1 output</td>
</tr>
<tr>
<td></td>
<td>CCP1</td>
<td>ST</td>
<td>CMOS</td>
<td>Capture input/Compare output/PWM output</td>
</tr>
<tr>
<td>GP1/AN1/CIN-/VREF/ICSPCLK</td>
<td>GP1</td>
<td>TTL</td>
<td>CMOS</td>
<td>GPIO I/O with prog. pull-up and interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>AN1</td>
<td>AN</td>
<td>—</td>
<td>A/D Channel 1 input</td>
</tr>
<tr>
<td></td>
<td>CIN-</td>
<td>AN</td>
<td>—</td>
<td>Comparator 1 input</td>
</tr>
<tr>
<td></td>
<td>VREF</td>
<td>AN</td>
<td>—</td>
<td>External Voltage Reference for A/D</td>
</tr>
<tr>
<td></td>
<td>ICSPCLK</td>
<td>ST</td>
<td>—</td>
<td>Serial Programming Clock</td>
</tr>
<tr>
<td>GP0/AN0/CIN+/ICSPDAT/ULPWU</td>
<td>GP0</td>
<td>TTL</td>
<td>CMOS</td>
<td>GPIO I/O with prog. pull-up and interrupt-on-change</td>
</tr>
<tr>
<td></td>
<td>AN0</td>
<td>AN</td>
<td>—</td>
<td>A/D Channel 0 input</td>
</tr>
<tr>
<td></td>
<td>CIN+</td>
<td>AN</td>
<td>—</td>
<td>Comparator 1 input</td>
</tr>
<tr>
<td></td>
<td>ICSPDAT</td>
<td>ST</td>
<td>CMOS</td>
<td>Serial Programming Data I/O</td>
</tr>
<tr>
<td></td>
<td>ULPWU</td>
<td>AN</td>
<td>—</td>
<td>Ultra Low-Power Wake-up input</td>
</tr>
<tr>
<td>Vss</td>
<td>Vss</td>
<td>Power</td>
<td>—</td>
<td>Ground reference</td>
</tr>
</tbody>
</table>

**Legend:**
- **AN** = Analog input or output
- **TTL** = TTL compatible input
- **ICSP** = ICSP compatible input or output
- **ST** = Schmitt Trigger input with CMOS levels
- **HV** = High Voltage
- **XTAL** = Crystal
- **CMOS** = CMOS compatible input or output
2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization
The PIC12F683 has a 13-bit program counter capable of addressing an 8k x 14 program memory space. Only the first 2k x 14 (0000h-07FFh) for the PIC12F683 is physically implemented. Accessing a location above these boundaries will cause a wraparound within the first 2K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F683

2.2 Data Memory Organization
The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-7Fh in Bank 0 and A0h-BFh in Bank 1 are General Purpose Registers, implemented as static RAM. Register locations F0h-FFh in Bank 1 point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read. RP0 of the STATUS register is the bank select bit.

RP0
0 → Bank 0 is selected
1 → Bank 1 is selected

Note: The IRP and RP1 bits of the STATUS register are reserved and should always be maintained as '0's.
2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 128 x 8 in the PIC12F683. Each register is accessed, either directly or indirectly, through the File Select Register FSR (see Section 2.4 “Indirect Addressing, INDF and FSR Registers”).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the “core” are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.
## TABLE 2-1: PIC12F683 SPECIAL REGISTERS SUMMARY BANK 0

<table>
<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>INDF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xx.xx xx.xx</td>
<td>17, 90</td>
</tr>
<tr>
<td>01h</td>
<td>TMR0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xx.xx xx.xx</td>
<td>41, 90</td>
</tr>
<tr>
<td>02h</td>
<td>PCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>17, 90</td>
</tr>
<tr>
<td>03h</td>
<td>STATUS</td>
<td>IRP(1)</td>
<td>RP1(1)</td>
<td>T0</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td></td>
<td>0001 1xxx</td>
<td>11, 90</td>
</tr>
<tr>
<td>04h</td>
<td>FSR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xx.xx xx.xx</td>
<td>17, 90</td>
</tr>
<tr>
<td>05h</td>
<td>GPIO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xx.xx xx.xx</td>
<td>31, 90</td>
</tr>
<tr>
<td>06h</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>07h</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>08h</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>09h</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0Ah</td>
<td>PCLATH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000 0000</td>
<td>13, 90</td>
</tr>
<tr>
<td>0Ch</td>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>CCP1IF</td>
<td>—</td>
<td>CMIF</td>
<td>OSIF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>000- 0000</td>
<td>15, 90</td>
</tr>
<tr>
<td>0Dh</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0Eh</td>
<td>TMR1L</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0Fh</td>
<td>TMR1H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>10h</td>
<td>T1CON</td>
<td>T1GINV</td>
<td>TMR1GE</td>
<td>T1CKPS1</td>
<td>T1CKPS0</td>
<td>T1OSCEN</td>
<td>TTSYNC</td>
<td>TMR1CS</td>
<td>TMR1ON</td>
<td>0000 0000</td>
<td>47, 90</td>
</tr>
<tr>
<td>11h</td>
<td>TMR2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>49, 90</td>
</tr>
<tr>
<td>12h</td>
<td>T2CON</td>
<td>TOUTPS3</td>
<td>TOUTPS2</td>
<td>TOUTPS1</td>
<td>TOUTPS0</td>
<td>TMR2ON</td>
<td>T2CKPS1</td>
<td>T2CKPS0</td>
<td>—</td>
<td>0000 0000</td>
<td>50, 90</td>
</tr>
<tr>
<td>13h</td>
<td>CCP1L</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>14h</td>
<td>CCP1H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>15h</td>
<td>CCP1CON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>75, 90</td>
</tr>
<tr>
<td>16h</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>17h</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>18h</td>
<td>WDTCON</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>19h</td>
<td>CMCON0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>COUT —</td>
<td>—</td>
</tr>
<tr>
<td>1Ah</td>
<td>CMCON1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CINV —</td>
<td>—</td>
</tr>
<tr>
<td>1Bh</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1Ch</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1Dh</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1Eh</td>
<td>ADRESH</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1Fh</td>
<td>ADCON0</td>
<td>ADFM</td>
<td>VCFG</td>
<td>CHS1</td>
<td>CHS0</td>
<td>GO/DONE</td>
<td>ADON</td>
<td></td>
<td></td>
<td>00-- 0000</td>
<td>65, 90</td>
</tr>
</tbody>
</table>

**Legend:**  
- = unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

**Note 1:** IRP and RP1 bits are reserved, always maintain these bits clear.
<table>
<thead>
<tr>
<th>Addr</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>80h</td>
<td>INDF</td>
<td>Addressing this location uses contents of FSR to address data memory (not a physical register)</td>
<td>xxxx</td>
<td>xxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>17, 90</td>
<td></td>
</tr>
<tr>
<td>81h</td>
<td>OPTION_REG</td>
<td>GPPU</td>
<td>INTEG</td>
<td>TOCS</td>
<td>TOSE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>1111 1111</td>
<td>12, 90</td>
</tr>
<tr>
<td>82h</td>
<td>PCL</td>
<td>Program Counter’s (PC) Least Significant Byte</td>
<td>0000</td>
<td>0000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>17, 90</td>
<td></td>
</tr>
<tr>
<td>83h</td>
<td>STATUS</td>
<td>IRP(1)</td>
<td>RP1(1)</td>
<td>RP0</td>
<td>T0</td>
<td>PD</td>
<td>Z</td>
<td>DC</td>
<td>C</td>
<td>0001</td>
<td>1xxx</td>
</tr>
<tr>
<td>84h</td>
<td>FSR</td>
<td>Indirect Data Memory Address Pointer</td>
<td>xxxx</td>
<td>xxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>17, 90</td>
<td></td>
</tr>
<tr>
<td>85h</td>
<td>TRISO</td>
<td>—</td>
<td>—</td>
<td>TRISI5</td>
<td>TRISI4</td>
<td>TRISI3</td>
<td>TRISI2</td>
<td>TRISI1</td>
<td>TRISI0</td>
<td>---11</td>
<td>1111</td>
</tr>
<tr>
<td>86h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>87h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>88h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>89h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>8Ah</td>
<td>PCLATH</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>8Bh</td>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>8Ch</td>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>CCP1IE</td>
<td>—</td>
<td>CMIE</td>
<td>OSIE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>8Dh</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>8 Eh</td>
<td>PCON</td>
<td>—</td>
<td>—</td>
<td>ULPWUE</td>
<td>SBOREN</td>
<td>—</td>
<td>—</td>
<td>POR</td>
<td>BOR</td>
<td>0011</td>
<td>--0</td>
</tr>
<tr>
<td>8Fh</td>
<td>OSCCON</td>
<td>—</td>
<td>IRCF2</td>
<td>IRCF1</td>
<td>IRCF0</td>
<td>OSTS(2)</td>
<td>HTS</td>
<td>LTS</td>
<td>SCS</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>90h</td>
<td>OSCTUNE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TUN4</td>
<td>TUN3</td>
<td>TUN2</td>
<td>TUN1</td>
<td>TUN0</td>
<td>0000</td>
</tr>
<tr>
<td>91h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>92h</td>
<td>PR2</td>
<td>Timer2 Module Period Register</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>49, 90</td>
</tr>
<tr>
<td>93h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>94h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>95h</td>
<td>WPU(3)</td>
<td>—</td>
<td>—</td>
<td>WPU5</td>
<td>WPU4</td>
<td>—</td>
<td>WPU2</td>
<td>WPU1</td>
<td>WPU0</td>
<td>0011</td>
<td>1111</td>
</tr>
<tr>
<td>96h</td>
<td>IOC</td>
<td>—</td>
<td>—</td>
<td>IOC5</td>
<td>IOC4</td>
<td>IOC3</td>
<td>IOC2</td>
<td>IOC1</td>
<td>IOC0</td>
<td>0011</td>
<td>1111</td>
</tr>
<tr>
<td>97h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>98h</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>99h</td>
<td>VRCON</td>
<td>VREN</td>
<td>—</td>
<td>VRR</td>
<td>—</td>
<td>VR3</td>
<td>VR2</td>
<td>VR1</td>
<td>VR0</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>9Ah</td>
<td>EEDAT</td>
<td>EEDAT7</td>
<td>EEDAT6</td>
<td>EEDAT5</td>
<td>EEDAT4</td>
<td>EEDAT3</td>
<td>EEDAT2</td>
<td>EEDAT1</td>
<td>EEDAT0</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>9Bh</td>
<td>EEADR</td>
<td>EEADR7</td>
<td>EEADR6</td>
<td>EEADR5</td>
<td>EEADR4</td>
<td>EEADR3</td>
<td>EEADR2</td>
<td>EEADR1</td>
<td>EEADR0</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>9Ch</td>
<td>EECON1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WRERR</td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
<td>0000</td>
<td>x000</td>
</tr>
<tr>
<td>9Dh</td>
<td>EECON2</td>
<td>EEPROM Control Register 2 (not a physical register)</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>——</td>
</tr>
<tr>
<td>9 Eh</td>
<td>ADRESL</td>
<td>Least Significant 2 bits of the left shifted result or 8 bits of the right shifted result</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>1111</td>
<td>66, 91</td>
</tr>
<tr>
<td>9Fh</td>
<td>ANSEL</td>
<td>—</td>
<td>—</td>
<td>ADCS2</td>
<td>ADCS1</td>
<td>ADCS0</td>
<td>ANS3</td>
<td>ANS2</td>
<td>ANS1</td>
<td>ANS0</td>
<td>——</td>
</tr>
</tbody>
</table>

**Legend:**
- = unimplemented locations read as ‘0’; u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

**Note 1:** IRP and RP1 bits are reserved, always maintain these bits clear.

**Note 2:** OSTS bit of the OSCCON register reset to ‘0’ with Dual Speed Start-up and LP, HS or XT selected as the oscillator.

**Note 3:** GP3 pull-up is enabled when MCLRE is ‘1’ in the Configuration Word register.
2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- Arithmetic status of the ALU
- Reset status
- Bank select bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS, will clear the upper three bits and set the Z bit. This leaves the STATUS register as 000u uulu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see the “Instruction Set Summary”.

Note 1: Bits IRP and RP1 of the STATUS register are not used by the PIC12F683 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.

2: The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction.

REGISTER 2-1: STATUS: STATUS REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>IRP</th>
<th>RP1</th>
<th>RP0</th>
<th>TO</th>
<th>PD</th>
<th>Z</th>
<th>DC</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td>Reserved</td>
<td>R/W-0</td>
<td>R-1</td>
<td>R-1</td>
<td>R/W-x</td>
<td>R/W-x</td>
<td>R/W-x</td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

bit 7 IRP: This bit is reserved and should be maintained as ‘0’
bit 6 RP1: This bit is reserved and should be maintained as ‘0’
bit 5 RP0: Register Bank Select bit (used for direct addressing)
  1 = Bank 1 (80h – FFh)
  0 = Bank 0 (00h – 7Fh)
bit 4 TO: Time-out bit
  1 = After power-up, CLRWDT instruction or SLEEP instruction
  0 = A WDT time-out occurred
bit 3 PD: Power-down bit
  1 = After power-up or by the CLRWDT instruction
  0 = By execution of the SLEEP instruction
bit 2 Z: Zero bit
  1 = The result of an arithmetic or logic operation is zero
  0 = The result of an arithmetic or logic operation is not zero
bit 1 DC: Digit Carry/Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions), For Borrow, the polarity is reversed.
  1 = A carry-out from the 4th low-order bit of the result occurred
  0 = No carry-out from the 4th low-order bit of the result
bit 0 C: Carry/Borrow bit(1) (ADDWF, ADDLW, SUBLW, SUBWF instructions)
  1 = A carry-out from the Most Significant bit of the result occurred
  0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For Borrow, the polarity is reversed. A subtraction is executed by adding the two’s complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.
2.2.2.2 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:
- TMR0/WDT prescaler
- External GP2/INT interrupt
- TMR0
- Weak pull-ups on GPIO

REGISTER 2-2: OPTION_REG: OPTION REGISTER

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
</tr>
</tbody>
</table>

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

bit 7
GPPU: GPIO Pull-up Enable bit
1 = GPIO pull-ups are disabled
0 = GPIO pull-ups are enabled by individual PORT latch values in WPU register

bit 6
INTEDG: Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

bit 5
T0CS: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4
T0SE: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3
PSA: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0
PS<2:0>: Prescaler Rate Select bits

<table>
<thead>
<tr>
<th>BIT VALUE</th>
<th>TIMER0 RATE</th>
<th>WDT RATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>1 : 2</td>
<td>1 : 1</td>
</tr>
<tr>
<td>001</td>
<td>1 : 4</td>
<td>1 : 2</td>
</tr>
<tr>
<td>010</td>
<td>1 : 8</td>
<td>1 : 4</td>
</tr>
<tr>
<td>011</td>
<td>1 : 16</td>
<td>1 : 8</td>
</tr>
<tr>
<td>100</td>
<td>1 : 32</td>
<td>1 : 16</td>
</tr>
<tr>
<td>101</td>
<td>1 : 64</td>
<td>1 : 32</td>
</tr>
<tr>
<td>110</td>
<td>1 : 128</td>
<td>1 : 64</td>
</tr>
<tr>
<td>111</td>
<td>1 : 256</td>
<td>1 : 128</td>
</tr>
</tbody>
</table>

Note: To achieve a 1:1 prescaler assignment for Timer0, assign the prescaler to the WDT by setting PSA bit of the OPTION register to ‘1’. See Section 5.1.3 “Software Programmable Prescaler”.

Note 1: A dedicated 16-bit WDT postscaler is available. See Section 12.6 “Watchdog Timer (WDT)” for more information.
2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, GPIO change and external GP2/INT pin interrupts.

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

---

### REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER

<table>
<thead>
<tr>
<th></th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

<table>
<thead>
<tr>
<th>bit 7</th>
<th>GIE: Global Interrupt Enable bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Enables all unmasked interrupts</td>
</tr>
<tr>
<td>0</td>
<td>Disables all interrupts</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 6</th>
<th>PEIE: Peripheral Interrupt Enable bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Enables all unmasked peripheral interrupts</td>
</tr>
<tr>
<td>0</td>
<td>Disables all peripheral interrupts</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 5</th>
<th>T0IE: Timer0 Overflow Interrupt Enable bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Enables the Timer0 interrupt</td>
</tr>
<tr>
<td>0</td>
<td>Disables the Timer0 interrupt</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 4</th>
<th>INTE: GP2/INT External Interrupt Enable bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Enables the GP2/INT external interrupt</td>
</tr>
<tr>
<td>0</td>
<td>Disables the GP2/INT external interrupt</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 3</th>
<th>GPIE: GPIO Change Interrupt Enable bit(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Enables the GPIO change interrupt</td>
</tr>
<tr>
<td>0</td>
<td>Disables the GPIO change interrupt</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 2</th>
<th>T0IF: Timer0 Overflow Interrupt Flag bit(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Timer0 register has overflowed (must be cleared in software)</td>
</tr>
<tr>
<td>0</td>
<td>Timer0 register did not overflow</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 1</th>
<th>INTF: GP2/INT External Interrupt Flag bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>The GP2/INT external interrupt occurred (must be cleared in software)</td>
</tr>
<tr>
<td>0</td>
<td>The GP2/INT external interrupt did not occur</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 0</th>
<th>GPIF: GPIO Change Interrupt Flag bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>When at least one of the GPIO &lt;5:0&gt; pins changed state (must be cleared in software)</td>
</tr>
<tr>
<td>0</td>
<td>None of the GPIO &lt;5:0&gt; pins have changed state</td>
</tr>
</tbody>
</table>

**Note 1:** IOC register must also be enabled.

**Note 2:** T0IF bit is set when TMR0 rolls over. TMR0 is unchanged on Reset and should be initialized before clearing T0IF bit.
2.2.2.4 PIE1 Register

The PIE1 register contains the interrupt enable bits, as shown in Register 2-4.

**REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1**

<table>
<thead>
<tr>
<th>Bit</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEIE</td>
<td>ADIE</td>
<td>CCP1IE</td>
<td>—</td>
<td>CMIE</td>
<td>OSFIE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7 EEIE**: EE Write Complete Interrupt Enable bit
  - 1 = Enables the EE write complete interrupt
  - 0 = Disables the EE write complete interrupt

- **bit 6 ADIE**: A/D Converter (ADC) Interrupt Enable bit
  - 1 = Enables the ADC interrupt
  - 0 = Disables the ADC interrupt

- **bit 5 CCP1IE**: CCP1 Interrupt Enable bit
  - 1 = Enables the CCP1 interrupt
  - 0 = Disables the CCP1 interrupt

- **bit 4 Unimplemented**: Read as ‘0’

- **bit 3 CMIE**: Comparator Interrupt Enable bit
  - 1 = Enables the Comparator 1 interrupt
  - 0 = Disables the Comparator 1 interrupt

- **bit 2 OSFIE**: Oscillator Fail Interrupt Enable bit
  - 1 = Enables the oscillator fail interrupt
  - 0 = Disables the oscillator fail interrupt

- **bit 1 TMR2IE**: Timer2 to PR2 Match Interrupt Enable bit
  - 1 = Enables the Timer2 to PR2 match interrupt
  - 0 = Disables the Timer2 to PR2 match interrupt

- **bit 0 TMR1IE**: Timer1 Overflow Interrupt Enable bit
  - 1 = Enables the Timer1 overflow interrupt
  - 0 = Disables the Timer1 overflow interrupt

**Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.
2.2.2.5 PIR1 Register

The PIR1 register contains the interrupt flag bits, as shown in Register 2-5.

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

### REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEIF</td>
<td>ADIF</td>
<td>CCP1IF</td>
<td>CMIF</td>
<td>OSFIF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 7 EEIF:** EEPROM Write Operation Interrupt Flag bit
- 1 = The write operation completed (must be cleared in software)
- 0 = The write operation has not completed or has not been started

**bit 6 ADIF:** A/D Interrupt Flag bit
- 1 = A/D conversion complete
- 0 = A/D conversion has not completed or has not been started

**bit 5 CCP1IF:** CCP1 Interrupt Flag bit
- **Capture mode:**
  - 1 = A TMR1 register capture occurred (must be cleared in software)
  - 0 = No TMR1 register capture occurred
- **Compare mode:**
  - 1 = A TMR1 register compare match occurred (must be cleared in software)
  - 0 = No TMR1 register compare match occurred
- **PWM mode:**
  - Unused in this mode

**bit 4 Unimplemented:** Read as ‘0’

**bit 3 CMIF:** Comparator Interrupt Flag bit
- 1 = Comparator 1 output has changed (must be cleared in software)
- 0 = Comparator 1 output has not changed

**bit 2 OSFIF:** Oscillator Fail Interrupt Flag bit
- 1 = System oscillator failed, clock input has changed to INTOSC (must be cleared in software)
- 0 = System clock operating

**bit 1 TMR2IF:** Timer2 to PR2 Match Interrupt Flag bit
- 1 = Timer2 to PR2 match occurred (must be cleared in software)
- 0 = Timer2 to PR2 match has not occurred

**bit 0 TMR1IF:** Timer1 Overflow Interrupt Flag bit
- 1 = Timer1 register overflowed (must be cleared in software)
- 0 = Timer1 has not overflowed
2.2.2.6 PCON Register

The Power Control (PCON) register contains flag bits (see Table 12-2) to differentiate between:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Watchdog Timer Reset (WDT)
- External MCLR Reset

The PCON register also controls the Ultra Low-Power Wake-up and software enable of the BOR.

The PCON register bits are shown in Register 2-6.

**REGISTER 2-6: PCON: POWER CONTROL REGISTER**

| bit 7-6 | Unimplemented: Read as ‘0’ |
| bit 5   | ULPWUE: Ultra Low-Power Wake-Up Enable bit |
|        | 1 = Ultra Low-Power Wake-up enabled |
|        | 0 = Ultra Low-Power Wake-up disabled |
| bit 4  | SBOREN: Software BOR Enable bit(1) |
|        | 1 = BOR enabled |
|        | 0 = BOR disabled |
| bit 3-2| Unimplemented: Read as ‘0’ |
| bit 1  | POR: Power-on Reset Status bit |
|        | 1 = No Power-on Reset occurred |
|        | 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs) |
| bit 0  | BOR: Brown-out Reset Status bit |
|        | 1 = No Brown-out Reset occurred |
|        | 0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs) |

**Note 1:** Set BOREN<1:0> = 01 in the Configuration Word register for this bit to control the BOR.
2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS

2.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note AN556, “Implementing a Table Read” (DS00556).

2.3.2 STACK

The PIC12F683 family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no Status bits to indicate stack overflow or stack underflow conditions.

Note 2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing. Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit of the STATUS register, as shown in Figure 2-4.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

MOVLW 0x20 ;initialize pointer
MOVWF FSR ;to RAM
NEXT CLR INDF ;clear INDF register
INC FSR ;inc pointer
BTFSS FSR,4 ;all done?
GOTO NEXT ;no clear next
CONTINUE ;yes continue
FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC12F683

For memory map detail, see Figure 2-2.

Note 1: The RP1 and IRP bits are reserved; always maintain these bits clear.
3.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

3.1 Overview

The Oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 3-1 illustrates a block diagram of the Oscillator module. Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured from one of two internal oscillators, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal via software.
- Two-Speed Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch automatically to the internal oscillator.

The Oscillator module can be configured in one of eight clock modes.

1. EC – External clock with I/O on OSC2/CLKOUT.
2. LP – 32 kHz Low-Power Crystal mode.
3. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
4. HS – High Gain Crystal or Ceramic Resonator mode.
5. RC – External Resistor-Capacitor (RC) with Fosc/4 output on OSC2/CLKOUT.
6. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
7. INTOSC – Internal oscillator with Fosc/4 output on OSC2 and I/O on OSC1/CLKIN.
8. INTOSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.

Clock Source modes are configured by the FOSC<2:0> bits in the Configuration Word register (CONFIG). The internal clock can be generated from two internal oscillators. The HFINTOSC is a calibrated high-frequency oscillator. The LFINTOSC is an uncalibrated low-frequency oscillator.

FIGURE 3-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM
## 3.2 Oscillator Control

The Oscillator Control (OSCCON) register (Figure 3-1) controls the system clock and frequency selection options. The OSCCON register contains the following bits:

- Frequency selection bits (IRCF)
- Frequency Status bits (HTS, LTS)
- System clock control bits (OSTS, SCS)

### REGISTER 3-1: OSCCON: OSCILLATOR CONTROL REGISTER

<table>
<thead>
<tr>
<th></th>
<th>U-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R-1</th>
<th>R-0</th>
<th>R-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>IRCF2</td>
<td>IRCF1</td>
<td>IRCF0</td>
<td>OSTS</td>
<td>HTS</td>
<td>LTS</td>
<td>SCS</td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- *x* = Bit is unknown

- **bit 7** Unimplemented: Read as ‘0’
- **bit 6-4** IRCF<2:0>: Internal Oscillator Frequency Select bits
  - 111 = 8 MHz
  - 110 = 4 MHz (default)
  - 101 = 2 MHz
  - 100 = 1 MHz
  - 011 = 500 kHz
  - 010 = 250 kHz
  - 001 = 125 kHz
  - 000 = 31 kHz (LFINTOSC)
- **bit 3** OSTS: Oscillator Start-up Time-out Status bit(1)
  - 1 = Device is running from the external clock defined by FOSC<2:0> of the Configuration Word register
  - 0 = Device is running from the internal oscillator (HFINTOSC or LFINTOSC)
- **bit 2** HTS: HFINTOSC Status bit (High Frequency – 8 MHz to 125 kHz)
  - 1 = HFINTOSC is stable
  - 0 = HFINTOSC is not stable
- **bit 1** LTS: LFINTOSC Stable bit (Low Frequency – 31 kHz)
  - 1 = LFINTOSC is stable
  - 0 = LFINTOSC is not stable
- **bit 0** SCS: System Clock Select bit
  - 1 = Internal oscillator is used for system clock
  - 0 = Clock source defined by FOSC<2:0> of the Configuration Word register

**Note 1:** Bit resets to ‘0’ with Two-Speed Start-up and LP, XT or HS selected as the Oscillator mode or Fail-Safe mode is enabled.
3.3 Clock Source Modes

Clock Source modes can be classified as external or internal.

- **External Clock modes** rely on external circuitry for the clock source. Examples are: Oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.
- **Internal clock sources** are contained internally within the Oscillator module. The Oscillator module has two internal oscillators: the 8 MHz High-Frequency Internal Oscillator (HFINTOSC) and the 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Select (SCS) bit of the OSCCON register. See Section 3.6 “Clock Switching” for additional information.

3.4 External Clock Modes

3.4.1 OSCILLATOR START-UP TIMER (OST)

If the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the Oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 3-1.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see Section 3.7 “Two-Speed Clock Start-up Mode”).

3.4.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 3-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.
3.4.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 3-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

**LP** Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

**XT** Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

**HS** Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 3-3 and Figure 3-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

**FIGURE 3-3:** QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)

- **Note 1:** A series resistor (Rs) may be required for quartz crystals with low drive level.
- **Note 2:** The value of Rs varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

**Note 1:** Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

- **Note 2:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.

- **Note 3:** For oscillator design assistance, reference the following Microchip Applications Notes:
  - AN826, “Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices” (DS00826)
  - AN849, “Basic PIC® Oscillator Design” (DS00849)
  - AN943, “Practical PIC® Oscillator Analysis and Design” (DS00943)
  - AN949, “Making Your Oscillator Work” (DS00949)

**FIGURE 3-4:** CERAMIC RESONATOR OPERATION (XT OR HS MODE)

- **Note 1:** A series resistor (Rs) may be required for ceramic resonators with low drive level.
- **Note 2:** The value of Rf varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).
- **Note 3:** An additional parallel feedback resistor (Rp) may be required for proper ceramic resonator operation.
### 3.4.4 EXTERNAL RC MODES

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes: RC and RCIO.

In RC mode, the RC circuit connects to OSC1. OSC2/CLKOUT outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 3-5 shows the external RC mode connections.

#### FIGURE 3-5: EXTERNAL RC MODES

In RCIO mode, the RC circuit is connected to OSC1. OSC1/CLKIN becomes an additional general purpose I/O pin.

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:
- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

### 3.5 Internal Clock Modes

The Oscillator module has two independent, internal oscillators that can be configured or selected as the system clock source.

1. **The HFINTOSC (High-Frequency Internal Oscillator)** is factory calibrated and operates at 8 MHz. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 3-2).

2. **The LFINTOSC (Low-Frequency Internal Oscillator)** is uncalibrated and operates at 31 kHz.

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits IRCF<2:0> of the OSCCON register.

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit of the OSCCON register. See Section 3.6 “Clock Switching” for more information.

#### 3.5.1 INTOSC AND INTOSCIO MODES

The INTOSC and INTOSCIO modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the FOSC<2:0> bits in the Configuration Word register (CONFIG). See Section 12.0 “Special Features of the CPU” for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTOSCIO** mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.

#### 3.5.2 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 8 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 3-2).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). One of seven frequencies can be selected via software using the IRCF<2:0> bits of the OSCCON register. See Section 3.5.4 “Frequency Select Bits (IRCF)” for more information.

The HFINTOSC is enabled by selecting any frequency between 8 MHz and 125 kHz by setting the IRCF<2:0> bits of the OSCCON register ≠ 000. Then, set the System Clock Source (SCS) bit of the OSCCON register to ‘1’ or enable Two-Speed Start-up by setting the IESO bit in the Configuration Word register (CONFIG) to ‘1’.

The HF Internal Oscillator (HTS) bit of the OSCCON register indicates whether the HFINTOSC is stable or not.
3.5.2.1 OSCTUNE Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-2).

The default value of the OSCTUNE register is ‘0’. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are not affected by the change in frequency.

REGISTER 3-2: OSCTUNE: OSCILLATOR TUNING REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>——</td>
<td>——</td>
<td>——</td>
<td>TUN4</td>
<td>TUN3</td>
<td>TUN2</td>
<td>TUN1</td>
<td>TUN0</td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**bit 7-5**

**Unimplemented:** Read as ‘0’

**bit 4-0**

**TUN<4:0>: Frequency Tuning bits**

- **01111** = Maximum frequency
- **01110** =
- **01101** =
- **01100** =
- **01011** =
- **01010** = Oscillator module is running at the calibrated frequency.
- **01001** =
- **01000** =
- **10001** =
- **10000** = Minimum frequency
3.5.3 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated 31 kHz internal clock source.

The output of the LFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). Select 31 kHz, via software, using the IRCF<2:0> bits of the OSCCON register. See Section 3.5.4 “Frequency Select Bits (IRCF)” for more information. The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF<2:0> bits of the OSCCON register = 000) as the system clock source (SCS bit of the OSCCON register = 1), or when any of the following are enabled:
- Two-Speed Start-up IESO bit of the Configuration Word register = 1 and IRCF<2:0> bits of the OSCCON register = 000
- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The LF Internal Oscillator (LTS) bit of the OSCCON register indicates whether the LFINTOSC is stable or not.

3.5.4 FREQUENCY SELECT BITS (IRCF)

The output of the 8 MHz HFINTOSC and 31 kHz LFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). The Internal Oscillator Frequency Select bits IRCF<2:0> of the OSCCON register select the frequency output of the internal oscillators. One of eight frequencies can be selected via software:
- 8 MHz
- 4 MHz (Default after Reset)
- 2 MHz
- 1 MHz
- 500 kHz
- 250 kHz
- 125 kHz
- 31 kHz (LFINTOSC)

**Note:** Following any Reset, the IRCF<2:0> bits of the OSCCON register are set to '110' and the frequency selection is set to 4 MHz. The user can modify the IRCF bits to select a different frequency.

3.5.5 HF AND LF INTOSC CLOCK SWITCH TIMING

When switching between the LFINTOSC and the HFINTOSC, the new oscillator may already be shut down to save power (see Figure 3-6). If this is the case, there is a delay after the IRCF<2:0> bits of the OSCCON register are modified before the frequency selection takes place. The LTS and HTS bits of the OSCCON register will reflect the current active status of the LFINTOSC and HFINTOSC oscillators. The timing of a frequency selection is as follows:
1. IRCF<2:0> bits of the OSCCON register are modified.
2. If the new clock is shut down, a clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. CLKOUT is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. CLKOUT is now connected with the new clock. LTS and HTS bits of the OSCCON register are updated as required.
6. Clock switch is complete.

See Figure 3-1 for more details.

If the internal oscillator speed selected is between 8 MHz and 125 kHz, there is no start-up delay before the new frequency is selected. This is because the old and new frequencies are derived from the HFINTOSC via the postscaler and multiplexer.

Start-up delay specifications are located in the Electrical Specifications Chapter of this data sheet, under AC Specifications (Oscillator Module).
FIGURE 3-6: INTERNAL OSCILLATOR SWITCH TIMING

HF → LF(1)
HFINTOSC → LFINTOSC (FSCM and WDT disabled)

HFINTOSC

Start-up Time

2-cycle Sync

Running

LFINTOSC

IRCF <2:0> ≠ 0 = 0

System Clock

Note 1: When going from LF to HF.

HFINTOSC → LFINTOSC (Either FSCM or WDT enabled)

HFINTOSC

2-cycle Sync

Running

LFINTOSC

IRCF <2:0> ≠ 0 = 0

System Clock

LFINTOSC turns off unless WDT or FSCM is enabled

 LFINTOSC

Start-up Time

2-cycle Sync

Running

HFINTOSC

IRCF <2:0> = 0 ≠ 0

System Clock
3.6 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bit of the OSCCON register.

3.6.1 SYSTEM CLOCK SELECT (SCS) BIT

The System Clock Select (SCS) bit of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bit of the OSCCON register = 0, the system clock source is determined by configuration of the FOSC<2:0> bits in the Configuration Word register (CONFIG).
- When the SCS bit of the OSCCON register = 1, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<2:0> bits of the OSCCON register. After a Reset, the SCS bit of the OSCCON register is always cleared.

Note: Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bit of the OSCCON register. The user can monitor the OSTS bit of the OSCCON register to determine the current system clock source.

3.6.2 OSCILLATOR START-UP TIME-OUT STATUS (OSTS) BIT

The Oscillator Start-up Time-out Status (OSTS) bit of the OSCCON register indicates whether the system clock is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes.

3.7 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.

This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

Note: Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCCON register to remain clear.

When the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) is enabled (see Section 3.4.1 “Oscillator Start-up Timer (OST)”). The OST will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as the OST is counting. When the OST count reaches 1024 and the OSTS bit of the OSCCON register is set, program execution switches to the external oscillator.

3.7.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Word register) = 1; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS (of the OSCCON register) = 0.
- FOSC<2:0> bits in the Configuration Word register (CONFIG) configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured to be anything other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

3.7.2 TWO-SPEED START-UP SEQUENCE

1. Wake-up from Power-on Reset or Sleep.
2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF<2:0> bits of the OSCCON register.
3. OST enabled to count 1024 clock cycles.
4. OST timed out, wait for falling edge of the internal oscillator.
5. OSTS is set.
6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
7. System clock is switched to external clock source.

Note: Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCCON register to remain clear.
3.7.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCCON register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or the internal oscillator.

FIGURE 3-7: TWO-SPEED START-UP

![Diagram showing two-speed start-up process](image-url)
3.8 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the Configuration Word register (CONFIG). The FSCM is applicable to all external oscillator modes (LP, XT, HS, EC, RC and RCIO).

FIGURE 3-8: FSCM BLOCK DIAGRAM

3.8.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 3-8. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the primary clock goes low.

3.8.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSFIF of the PIR1 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE1 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation.

The internal clock source chosen by the FSCM is determined by the IRCF<2:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.

3.8.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or toggling the SCS bit of the OSCCON register. When the SCS bit is toggled, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared and the device will be operating from the external clock source. The Fail-Safe condition must be cleared before the OSFIF flag can be cleared.

3.8.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC or RC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. When the FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, the device will always be executing code while the OST is operating.

Note: Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the OSTS bit of the OSCCON register to verify the oscillator start-up and that the system clock switchover has successfully completed.
FIGURE 3-9: FSCM TIMING DIAGRAM

Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG(2)</td>
<td>CPD</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWRT</td>
<td>WDTE</td>
<td>FOSC2</td>
<td>FOSC1</td>
<td>FOSC0</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>OSCCON</td>
<td>—</td>
<td>IRCF2</td>
<td>IRCF1</td>
<td>IRCF0</td>
<td>OSTS</td>
<td>HTS</td>
<td>LTS</td>
<td>SCS</td>
<td>-110 x000</td>
<td>-110 x000</td>
</tr>
<tr>
<td>OSCTUNE</td>
<td>—</td>
<td>—</td>
<td>TUN4</td>
<td>TUN3</td>
<td>TUN2</td>
<td>TUN1</td>
<td>TUN0</td>
<td>—</td>
<td>---0 0000</td>
<td>---u uuuuu</td>
</tr>
<tr>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>CCP1IE</td>
<td>—</td>
<td>CMIE</td>
<td>OSFIE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>000- 0000</td>
<td>000- 0000</td>
</tr>
<tr>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>CCP1IF</td>
<td>—</td>
<td>CMIF</td>
<td>OSIF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>000- 0000</td>
<td>000- 0000</td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented locations read as ‘0’. Shaded cells are not used by oscillators.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: See Configuration Word register (Register 12-1) for operation of all register bits.
4.0  GPIO PORT

There are as many as six general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

4.1  GPIO and the TRISIO Registers

GPIO is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISIO. Setting a TRISIO bit (= 1) will make the corresponding GPIO pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISIO bit (= 0) will make the corresponding GPIO pin an output (i.e., put the contents of the output latch on the selected pin). An exception is GP3, which is input only and its TRISIO bit will always read as '1'. Example 4-1 shows how to initialize GPIO.

Reading the GPIO register reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations.

Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. GP3 reads ‘0’ when MCLR = 1.

The TRISIO register controls the direction of the GPIO pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISIO register are maintained set when using them as analog inputs. I/O pins configured as analog input always read ‘0’.

Note: The ANSEL and CMCON0 registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’.

EXAMPLE 4-1: INITIALIZING GPIO

```
BANKSEL GPIO ;
CLRF GPIO ; Init GPIO
MOVLW 07h ; Set GP<2:0> to digital I/O
MOVWF CMCON0 ;
BANKSEL ANSEL ;
CLRF ANSEL ;
MOVLW 0Ch ; Set GP<3:2> as inputs
MOVWF TRISIO ;
                 ; and set GP<5:4,1:0> as outputs
```

REGISTER 4-1: GPIO: GENERAL PURPOSE I/O REGISTER

| bit 7-6 | Unimplemented: Read as ‘0’ |
| bit 5-0 | GP<5:0>: GPIO I/O Pin bit |
|         | 1 = Port pin is > Vih |
|         | 0 = Port pin is < VIL |

Legend: 
R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
- U = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown

© 2007 Microchip Technology Inc.  DS41211D-page 31
4.2 Additional Pin Functions

Every GPIO pin on the PIC12F683 has an interrupt-on-change option and a weak pull-up option. GP0 has an Ultra Low-Power Wake-up option. The next three sections describe these functions.

4.2.1 ANSEL REGISTER

The ANSEL register is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSEL bit high will cause all digital reads on the pin to be read as ‘0’ and allow analog functions on the pin to operate correctly.

The state of the ANSEL bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

4.2.2 WEAK PULL-UPS

Each of the GPIO pins, except GP3, has an individually configurable internal weak pull-up. Control bits WPUx enable or disable each pull-up. Refer to Register 4-4. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the GPPU bit of the OPTION register. A weak pull-up is automatically enabled for GP3 when configured as MCLR and disabled when GP3 is an I/O. There is no software control of the MCLR pull-up.

4.2.3 INTERRUPT-ON-CHANGE

Each of the GPIO pins is individually configurable as an interrupt-on-change pin. Control bits IOCx enable or disable the interrupt function for each pin. Refer to Register 4-5. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of GPIO. The ‘mismatch’ outputs of the last read are OR’d together to set the GPIO Change Interrupt Flag bit (GPIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read or write of GPIO. This will end the mismatch condition, then,

b) Clear the flag bit GPIF.

A mismatch condition will continue to set flag bit GPIF. Reading GPIO will end the mismatch condition and allow flag bit GPIF to be cleared. The latch holding the last read value is not affected by a MCLR nor Brown-out Reset. After these resets, the GPIF flag will continue to be set if a mismatch is present.

Note: If a change on the I/O pin should occur when any GPIO operation is being executed, then the GPIF interrupt flag may not get set.
**REGISTER 4-3: ANSEL: ANALOG SELECT REGISTER**

<table>
<thead>
<tr>
<th>bit 7-0</th>
<th>Unimplemented: Read as '0'</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 6-4</td>
<td>ADCS&lt;2:0&gt;: A/D Conversion Clock Select bits</td>
</tr>
<tr>
<td>000</td>
<td>FOSC/2</td>
</tr>
<tr>
<td>001</td>
<td>FOSC/8</td>
</tr>
<tr>
<td>010</td>
<td>FOSC/32</td>
</tr>
<tr>
<td>x11</td>
<td>FRC (clock derived from a dedicated internal oscillator = 500 kHz max)</td>
</tr>
<tr>
<td>100</td>
<td>FOSC/4</td>
</tr>
<tr>
<td>101</td>
<td>FOSC/16</td>
</tr>
<tr>
<td>110</td>
<td>FOSC/64</td>
</tr>
<tr>
<td>bit 3-0</td>
<td>ANS&lt;3:0&gt;: Analog Select bits</td>
</tr>
<tr>
<td>1</td>
<td>Analog input. Pin is assigned as analog input(1).</td>
</tr>
<tr>
<td>0</td>
<td>Digital I/O. Pin is assigned to port or special function.</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**Note 1:** Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups and interrupt-on-change, if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.
### REGISTER 4-4: WPU: WEAK PULL-UP REGISTER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>U-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>WPU5</td>
<td>WPU4</td>
<td>—</td>
<td>WPU2</td>
<td>WPU1</td>
<td>WPU0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- **bit 7-6** Unimplemented: Read as ‘0’
- **bit 5-4** WPU<5:4>: Weak Pull-up Control bits
  - 1 = Pull-up enabled
  - 0 = Pull-up disabled
- **bit 3** Unimplemented: Read as ‘0’
- **bit 2-0** WPU<2:0>: Weak Pull-up Control bits
  - 1 = Pull-up enabled
  - 0 = Pull-up disabled

**Note 1:** Global GPPU must be enabled for individual pull-ups to be enabled.
**Note 2:** The weak pull-up device is automatically disabled if the pin is in Output mode (TRISIO = 0).
**Note 3:** The GP3 pull-up is enabled when configured as MCLR and disabled as an I/O in the Configuration Word.
**Note 4:** WPU<5:4> always reads ‘1’ in XT, HS and LP OSC modes.

### REGISTER 4-5: IOC: INTERRUPT-ON-CHANGE GPIO REGISTER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>IOC5</td>
<td>IOC4</td>
<td>IOC3</td>
<td>IOC2</td>
<td>IOC1</td>
<td>IOC0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- **bit 7-6** Unimplemented: Read as ‘0’
- **bit 5-0** IOC<5:0>: Interrupt-on-change GPIO Control bits
  - 1 = Interrupt-on-change enabled
  - 0 = Interrupt-on-change disabled

**Note 1:** Global Interrupt Enable (GIE) must be enabled for individual interrupts to be recognized.
**Note 2:** IOC<5:4> always reads ‘0’ in XT, HS and LP OSC modes.
4.2.4  ULTRA LOW-POWER WAKE-UP

The Ultra Low-Power Wake-up (ULPWU) on GP0 allows a slow falling voltage to generate an interrupt-on-change on GP0 without excess current consumption. The mode is selected by setting the ULPWUE bit of the PCON register. This enables a small current sink which can be used to discharge a capacitor on GP0.

To use this feature, the GP0 pin is configured to output ‘1’ to charge the capacitor, interrupt-on-change for GP0 is enabled and GP0 is configured as an input. The ULPWUE bit is set to begin the discharge and a SLEEP instruction is performed. When the voltage on GP0 drops below VIL, an interrupt will be generated which will cause the device to wake-up. Depending on the state of the GIE bit of the INTCON register, the device will either jump to the interrupt vector (0004h) or execute the next instruction when the interrupt event occurs. See Section 4.2.3 “Interrupt-on-Change” and Section 12.4.3 “GPIO Interrupt” for more information.

This feature provides a low-power technique for periodically waking up the device from Sleep. The time-out is dependent on the discharge time of the RC circuit on GP0. See Example 4-2 for initializing the Ultra Low-Power Wake-up module.

The series resistor provides overcurrent protection for the GP0 pin and can allow for software calibration of the time-out (see Figure 4-1). A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired interrupt delay. This technique will compensate for the affects of temperature, voltage and component accuracy. The Ultra Low-Power Wake-up peripheral can also be configured as a simple Programmable Low-Voltage Detect or temperature sensor.

Note: For more information, refer to the Application Note AN879, “Using the Microchip Ultra Low-Power Wake-up Module” (DS00879).

EXAMPLE 4-2: ULTRA LOW-POWER WAKE-UP INITIALIZATION

Note: For more information, refer to the Applica- tion Note AN879, “Using the Microchip Ultra Low-Power Wake-up Module” (DS00879).

BANKSEL CMCON0 ;
MOVLW H’7’ ;Turn off
MOVWF CMCON0 ;comparators
BANKSEL ANSEL ;
BCF ANSEL,0 ;RA0 to digital I/O
BCF TRISA,0 ;Output high to
BANKSEL PORTA ;
BSF PORTA,0 ;charge capacitor
CALL CapDelay ;
BANKSEL PCON ;
BSF PCON,ULPWUE ;Enable ULP Wake-up
BSF IOCA,0 ;Select RA0 IOC
BSF TRISA,0 ;RA0 to input
MOVLW B’10001000’ ;Enable interrupt
MOVWF INTCON ; and clear flag
SLEEP ;Wait for IOC
NOP ;
4.2.5 PIN DESCRIPTIONS AND DIAGRAMS

Each GPIO pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the ADC, refer to the appropriate section in this data sheet.

4.2.5.1 GP0/AN0/CIN+/ICSPDAT/ULPWU

Figure 4-1 shows the diagram for this pin. The GP0 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog input to the comparator
- In-Circuit Serial Programming™ data
- an analog input to the Ultra Low-Power Wake-up

FIGURE 4-1: BLOCK DIAGRAM OF GP0

Note 1: Comparator mode and ANSEL determines Analog Input mode.
4.2.5.2 GP1/AN1/CIN-/VREF/ICSPCLK

Figure 4-2 shows the diagram for this pin. The GP1 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a voltage reference input for the ADC
- In-Circuit Serial Programming clock

**FIGURE 4-2: BLOCK DIAGRAM OF GP1**

4.2.5.3 GP2/AN2/T0CKI/INT/COUT/CCP1

Figure 4-3 shows the diagram for this pin. The GP2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- the clock input for Timer0
- an external edge triggered interrupt
- a digital output from the Comparator
- a digital input/output for the CCP (refer to Section 11.0 “Capture/Compare/PWM (CCP) Module”).

**FIGURE 4-3: BLOCK DIAGRAM OF GP2**

**Note 1:** Comparator mode and ANSEL determines Analog Input mode.
4.2.5.4 GP3/MCLR/VPP

Figure 4-4 shows the diagram for this pin. The GP3 pin is configurable to function as one of the following:

- a general purpose input
- as Master Clear Reset with weak pull-up

**FIGURE 4-4: BLOCK DIAGRAM OF GP3**

4.2.5.5 GP4/AN3/T1G/OSC2/CLKOUT

Figure 4-5 shows the diagram for this pin. The GP4 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a Timer1 gate input
- a crystal/resonator connection
- a clock output

**FIGURE 4-5: BLOCK DIAGRAM OF GP4**

*Note 1:* CLK modes are XT, HS, LP, optional LP oscillator and CLKOUT Enable.
*Note 2:* With CLKOUT option.
4.2.5.6 GP5/T1CKI/OSC1/CLKIN

Figure 4-6 shows the diagram for this pin. The GP5 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 clock input
- a crystal/resonator connection
- a clock input

FIGURE 4-6: BLOCK DIAGRAM OF GP5

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH GPIO

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSEL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ADCS2 – ADCS1 – ADCS0</td>
<td>ANS3 – ANS2 – ANS1 – ANS0</td>
</tr>
<tr>
<td>CCP1CON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>DC1B1 – DC1B0 – CC1M3</td>
<td>CCP1M2 – CCP1M1 – CCP1M0</td>
</tr>
<tr>
<td>CMCON0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>COUT – CINV – CIS – CM2</td>
<td>CM1 – CM0</td>
</tr>
<tr>
<td>PCON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ULPWUE – SBREN – POR</td>
<td>BOR</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000 0000 – 0000 0000x</td>
<td>0000 0000 – 0000 0000x</td>
</tr>
<tr>
<td>IOC</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IOCS – IOCS – IOC3 – IOC2</td>
<td>IOC1 – IOC0</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>GPPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>1111 1111 – 1111 1111</td>
<td>1111 1111 – 1111 1111</td>
</tr>
<tr>
<td>GPIO</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>GP5 – GP4 – GP3 – GP2</td>
<td>GP1 – GP0</td>
</tr>
<tr>
<td>T1CON</td>
<td>T1GINV</td>
<td>TMR1GE</td>
<td>T1CKPS1</td>
<td>T1CKPS0</td>
<td>T1OSCEN</td>
<td>T1SYNC</td>
<td>TMR1CS</td>
<td>TMR1CON</td>
<td>0000 0000 – 0000 0000</td>
<td>0000 0000 – 0000 0000</td>
</tr>
<tr>
<td>TRISIO</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>TRISIO5</td>
<td>TRISIO4</td>
<td>TRISIO3</td>
<td>TRISIO2</td>
<td>TRISIO1 – TRISIO0</td>
<td>--11 1111 – --11 1111</td>
</tr>
<tr>
<td>WPU</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WP5</td>
<td>WP4</td>
<td>—</td>
<td>WP2</td>
<td>WPU2 – WPU1 – WPU0</td>
<td>--11 -111 – --11 -111</td>
</tr>
</tbody>
</table>

Legend:  
- x = unknown, u = unchanged, - = unimplemented locations read as ‘0’. Shaded cells are not used by GPIO.
5.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (shared with Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow

Figure 5-1 is a block diagram of the Timer0 module.

5.1 Timer0 Operation

When used as a timer, the Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

5.1.1 8-BIT TIMER MODE

When used as a timer, the Timer0 module will increment every instruction cycle (without prescaler). Timer mode is selected by clearing the T0CS bit of the OPTION register to ‘0’.

When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note: The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

5.1.2 8-BIT COUNTER MODE

When used as a counter, the Timer0 module will increment on every rising or falling edge of the T0CKI pin. The incrementing edge is determined by the T0SE bit of the OPTION register. Counter mode is selected by setting the T0CS bit of the OPTION register to ‘1’.

FIGURE 5-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.
2: SWDTEN and WDTPS<3:0> are bits in the WDTCON register.
3: WDTE bit is in the Configuration Word register.
5.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A single software programmable prescaler is available for use with either Timer0 or the Watchdog Timer (WDT), but not both simultaneously. The prescaler assignment is controlled by the PSA bit of the OPTION register. To assign the prescaler to Timer0, the PSA bit must be cleared to a '0'.

There are 8 prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be assigned to the WDT module.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler.

When the prescaler is assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

5.1.3.1 Switching Prescaler Between Timer0 and WDT Modules

As a result of having the prescaler assigned to either Timer0 or the WDT, it is possible to generate an unintended device Reset when switching prescaler values. When changing the prescaler assignment from Timer0 to the WDT module, the instruction sequence shown in Example 5-1, must be executed.

EXAMPLE 5-1: CHANGING PRESCALER (TIMER0 → WDT)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BANKSEL TMR0 ;</td>
<td>Select TMR0 bank</td>
</tr>
<tr>
<td>CLR WDT ;</td>
<td>Clear WDT</td>
</tr>
<tr>
<td>CLRF TMR0 ;</td>
<td>Clear TMR0 and prescaler</td>
</tr>
<tr>
<td>BANKSEL OPTION_REG ;</td>
<td>Select OPTION_REG bank</td>
</tr>
<tr>
<td>BSF OPTION_REG, PSA ;</td>
<td>Select WDT</td>
</tr>
<tr>
<td>CLRWDT ;</td>
<td>Clear prescaler</td>
</tr>
<tr>
<td>MOV L W b’11110000’ ;</td>
<td>Mask prescaler</td>
</tr>
<tr>
<td>ANDWF OPTION_REG,W ;</td>
<td>Set prescaler bits</td>
</tr>
<tr>
<td>IORLW b’00000011’ ;</td>
<td>Set WDT prescaler</td>
</tr>
<tr>
<td>MOVWF OPTION_REG ;</td>
<td>Set prescaler to 1:16</td>
</tr>
</tbody>
</table>

When changing the prescaler assignment from the WDT to the Timer0 module, the following instruction sequence must be executed (see Example 5-2).

EXAMPLE 5-2: CHANGING PRESCALER (WDT → TIMER0)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLRWDT ;</td>
<td>Clear WDT and prescaler</td>
</tr>
<tr>
<td>BANKSEL OPTION_REG ;</td>
<td>Select OPTION_REG bank</td>
</tr>
<tr>
<td>MOV L W b’11110000’ ;</td>
<td>Mask TMR0 select and prescaler</td>
</tr>
<tr>
<td>ANDWF OPTION_REG,W ;</td>
<td>Set prescaler bits</td>
</tr>
<tr>
<td>IORLW b’00000011’ ;</td>
<td>Set prescale to 1:16</td>
</tr>
<tr>
<td>MOVWF OPTION_REG ;</td>
<td>Set prescaler to 1:16</td>
</tr>
</tbody>
</table>

5.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The TOIF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The TOIF bit must be cleared in software. The Timer0 interrupt enable is the T0IE bit of the INTCON register.

Note: The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.

5.1.5 USING TIMER0 WITH AN EXTERNAL CLOCK

When Timer0 is in Counter mode, the synchronization of the T0CKI input and the Timer0 register is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, the high and low periods of the external clock source must meet the timing requirements as shown in the Section 15.0 “Electrical Specifications”.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLRWDT ;</td>
<td>Clear WDT and prescaler</td>
</tr>
<tr>
<td>BANKSEL OPTION_REG ;</td>
<td>Select OPTION_REG bank</td>
</tr>
<tr>
<td>MOV L W b’11110000’ ;</td>
<td>Mask TMR0 select and prescaler</td>
</tr>
<tr>
<td>ANDWF OPTION_REG,W ;</td>
<td>Set prescaler bits</td>
</tr>
<tr>
<td>IORLW b’00000011’ ;</td>
<td>Set prescale to 1:16</td>
</tr>
<tr>
<td>MOVWF OPTION_REG ;</td>
<td>Set prescaler to 1:16</td>
</tr>
</tbody>
</table>
TABLE 5-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

### REGISTER 5-1: OPTION_REG: OPTION REGISTER

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit  
- W = Writable bit  
- U = Unimplemented bit, read as ‘0’  
- -n = Value at POR  
- ‘1’ = Bit is set  
- ‘0’ = Bit is cleared  
- x = Bit is unknown

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
</table>
| **GPPU**: GPIO Pull-up Enable bit  
1 = GPIO pull-ups are disabled  
0 = GPIO pull-ups are enabled by individual PORT latch values in WPU register
| **INTEDG**: Interrupt Edge Select bit  
1 = Interrupt on rising edge of INT pin  
0 = Interrupt on falling edge of INT pin
| **T0CS**: Timer0 Clock Source Select bit  
1 = Transition on T0CKI pin  
0 = Internal instruction cycle clock (Fosc/4)
| **T0SE**: Timer0 Source Edge Select bit  
1 = Increment on high-to-low transition on T0CKI pin  
0 = Increment on low-to-high transition on T0CKI pin
| **PSA**: Prescaler Assignment bit  
1 = Prescaler is assigned to the WDT  
0 = Prescaler is assigned to the Timer0 module
| **PS<2:0>**: Prescaler Rate Select bits

<table>
<thead>
<tr>
<th>BIT VALUE</th>
<th>TIMER0 RATE</th>
<th>WDT RATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>1 : 2</td>
<td>1 : 1</td>
</tr>
<tr>
<td>001</td>
<td>1 : 4</td>
<td>1 : 2</td>
</tr>
<tr>
<td>010</td>
<td>1 : 8</td>
<td>1 : 4</td>
</tr>
<tr>
<td>011</td>
<td>1 : 16</td>
<td>1 : 8</td>
</tr>
<tr>
<td>100</td>
<td>1 : 32</td>
<td>1 : 16</td>
</tr>
<tr>
<td>101</td>
<td>1 : 64</td>
<td>1 : 32</td>
</tr>
<tr>
<td>110</td>
<td>1 : 128</td>
<td>1 : 64</td>
</tr>
<tr>
<td>111</td>
<td>1 : 256</td>
<td>1 : 128</td>
</tr>
</tbody>
</table>

**Note 1:** A dedicated 16-bit WDT postscaler is available. See Section 12.6 “Watchdog Timer (WDT)” for more information.
6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:
- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 3-bit prescaler
- Optional LP oscillator
- Synchronous or asynchronous operation
- Timer1 gate (count enable) via comparator or T1G pin
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Special Event Trigger (with CCP)
- Comparator output synchronization to Timer1 clock

Figure 6-1 is a block diagram of the Timer1 module.

6.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer. When used with an external clock source, the module can be used as either a timer or counter.

6.2 Clock Source Selection

The TMR1CS bit of the T1CON register is used to select the clock source. When TMR1CS = 0, the clock source is Fosc/4. When TMR1CS = 1, the clock source is supplied externally.

<table>
<thead>
<tr>
<th>Clock Source</th>
<th>TMR1CS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fosc/4</td>
<td>0</td>
</tr>
<tr>
<td>T1CKI pin</td>
<td>1</td>
</tr>
</tbody>
</table>

Note 1: ST Buffer is low power type when using LP oscillator, or high speed type when using T1CKI.
Note 2: Timer1 register increments on rising edge.
Note 3: Synchronize does not operate while in Sleep.
6.2.1 INTERNAL CLOCK SOURCE
When the internal clock source is selected the TMR1H:TMR1L register pair will increment on multiples of TCy as determined by the Timer1 prescaler.

6.2.2 EXTERNAL CLOCK SOURCE
When the external clock source is selected, the Timer1 module may work as a timer or a counter. When counting, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously. If an external clock oscillator is needed (and the microcontroller is using the INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge.

6.3 Timer1 Prescaler
Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

6.4 Timer1 Oscillator
A low-power 32.768 kHz crystal oscillator is built-in between pins OSC1 (input) and OSC2 (amplifier output). The oscillator is enabled by setting the T1OSCEN control bit of the T1CON register. The oscillator will continue to run during Sleep. The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is derived from the internal oscillator or when in LP oscillator mode. The user must provide a software time delay to ensure proper oscillator start-up.

TRISIO<5:4> bits are set when the Timer1 oscillator is enabled. GP5 and GP4 bits read as ‘0’ and TRISIO5 and TRISIO4 bits read as ‘1’.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

6.5 Timer1 Operation in Asynchronous Counter Mode
If control bit T1SYNC of the T1CON register is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see Section 6.5.1 “Reading and Writing Timer1 in Asynchronous Counter Mode”).

Note: When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce a single spurious increment.

6.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE
Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

6.6 Timer1 Gate
Timer1 gate source is software configurable to be the T1G pin or the output of the Comparator. This allows the device to directly time external events using T1G or analog events using Comparator 2. See the CMCON1 register (Register 8-2) for selecting the Timer1 gate source. This feature can simplify the software for a Delta-Sigma A/D converter and many other applications. For more information on Delta-Sigma A/D converters, see the Microchip web site (www.microchip.com).

Note: TMR1GE bit of the T1CON register must be set to use either T1G or COUT as the Timer1 gate source. See Register 8-2 for more information on selecting the Timer1 gate source.

Timer1 gate can be inverted using the T1GINV bit of the T1CON register, whether it originates from the T1G pin or Comparator 2 output. This configures Timer1 to measure either the active-high or active-low time between events.
6.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:
- Timer1 interrupt enable bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

6.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:
- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set

The device will wake-up on an overflow and execute the next instruction. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

6.9 CCP Special Event Trigger

If a CCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer1.

Timer1 should be synchronized to the Fosc to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the CCP, the write will take precedence.

For more information, see Section on CCP.

6.10 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see Section 8.0 “Comparator Module”.

Note: The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

FIGURE 6-2: TIMER1 INCREMENTING EDGE

T1CKI = 1 when TMR1 Enabled

T1CKI = 0 when TMR1 Enabled

Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.
6.11 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 6-1, is used to control Timer1 and select the various features of the Timer1 module.

**REGISTER 6-1: T1CON: TIMER1 CONTROL REGISTER**

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1GINV(1)</td>
<td>TMR1GE(2)</td>
<td>T1CKPS1</td>
<td>T1CKPS0</td>
<td>T1OSCEN</td>
<td>T1SYNC</td>
<td>TMR1CS</td>
<td>TMR1ON</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

- **bit 7 T1GINV: Timer1 Gate Invert bit(1)**
  - 1 = Timer1 gate is active-high (Timer1 counts when gate is high)
  - 0 = Timer1 gate is active-low (Timer1 counts when gate is low)

- **bit 6 TMR1GE: Timer1 Gate Enable bit(2)**
  - If TMR1ON = 0:
    - This bit is ignored
  - If TMR1ON = 1:
    - 1 = Timer1 is on if Timer1 gate is not active
    - 0 = Timer1 is on

- **bit 5-4 T1CKPS<1:0>: Timer1 Input Clock Prescale Select bits**
  - 11 = 1:8 Prescale Value
  - 10 = 1:4 Prescale Value
  - 01 = 1:2 Prescale Value
  - 00 = 1:1 Prescale Value

- **bit 3 T1OSCEN: LP Oscillator Enable Control bit**
  - If INTOSC without CLKOUT oscillator is active:
    - 1 = LP oscillator is enabled for Timer1 clock
    - 0 = LP oscillator is off
  - Else:
    - This bit is ignored. LP oscillator is disabled.

- **bit 2 T1SYNC: Timer1 External Clock Input Synchronization Control bit**
  - **TMR1CS** = 1:
    - 1 = Do not synchronize external clock input
    - 0 = Synchronize external clock input
  - **TMR1CS** = 0:
    - This bit is ignored. Timer1 uses the internal clock

- **bit 1 TMR1CS: Timer1 Clock Source Select bit**
  - 1 = External clock from T1CKI pin (on the rising edge)
  - 0 = Internal clock (FOSC/4)

- **bit 0 TMR1ON: Timer1 On bit**
  - 1 = Enables Timer1
  - 0 = Stops Timer1

**Note 1:** T1GINV bit inverts the Timer1 gate logic, regardless of source.

**Note 2:** TMR1GE bit must be set to use either T1G pin or COUT, as selected by the T1GSS bit of the CMCON1 register, as a Timer1 gate source.
### TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG</td>
<td>CPD</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWRT</td>
<td>WDTE</td>
<td>FOSC2</td>
<td>FOSC1</td>
<td>FOSC0</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>CMCON1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>T1GSS</td>
<td>CMSYNC</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0F</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000 0000</td>
<td>0000 0000x</td>
</tr>
<tr>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>CCP1IE</td>
<td>—</td>
<td>CMIE</td>
<td>OSFIE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>CCP1IF</td>
<td>—</td>
<td>CMIF</td>
<td>OSFIF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>TMR1H</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>TMR1L</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>T1CON</td>
<td>T1GINV</td>
<td>TMR1GE</td>
<td>T1CKPS1</td>
<td>T1CKPS0</td>
<td>T1OSCEN</td>
<td>T1SYNC</td>
<td>TMR1CS</td>
<td>TMR1ON</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
</tbody>
</table>

**Legend:**
- x = unknown, u = unchanged, – = unimplemented, read as ‘0’. Shaded cells are not used by the Timer1 module.

**Note 1:** See Configuration Word register (Register 12-1) for operation of all register bits.
7.0 TIMER2 MODULE

The Timer2 module is an 8-bit timer with the following features:
- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)

See Figure 7-1 for a block diagram of Timer2.

7.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock (Fosc/4). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:
- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented

The match output of the Timer2/PR2 comparator is then fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a ‘1’. Timer2 is turned off by clearing the TMR2ON bit to a ‘0’.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:
- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, MCLR Reset, Watchdog Timer Reset, or Brown-out Reset).

Note: TMR2 is not cleared when T2CON is written.
TABLE 7-1: SUMMARY OF ASSOCIATED TIMER2 REGISTERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GIE</td>
<td>T0IF</td>
<td>INTE</td>
<td>GIE</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>CP1IE</td>
<td>INTIE</td>
<td>CMIE</td>
<td>OSFIE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>000- 0000</td>
<td>000- 0000</td>
</tr>
<tr>
<td>PIR1</td>
<td>EEIE</td>
<td>ADIF</td>
<td>CP1IF</td>
<td>CMIF</td>
<td>OSFIF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td></td>
<td>000- 0000</td>
<td>000- 0000</td>
</tr>
<tr>
<td>PR2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
<tr>
<td>TMR2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>T2CON</td>
<td></td>
<td>TOUTPS3</td>
<td>TOUTPS2</td>
<td>TOUTPS1</td>
<td>TOUTPS0</td>
<td>TMR2ON</td>
<td>T2CKPS1</td>
<td>T2CKPS0</td>
<td>-000 0000</td>
<td>-000 0000</td>
</tr>
</tbody>
</table>

Legend:  
- x = unknown, u = unchanged, - = unimplemented read as ‘0’. Shaded cells are not used for Timer2 module.
8.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The comparators are very useful mixed signal building blocks because they provide analog functionality independent of the program execution. The analog comparator module includes the following features:

- Multiple comparator configurations
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Timer1 gate (count enable)
- Output synchronization to Timer1 clock input
- Programmable voltage reference

8.1 Comparator Overview

The comparator is shown in Figure 8-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at \( V_{IN+} \) is less than the analog voltage at \( V_{IN-} \), the output of the comparator is a digital low level. When the analog voltage at \( V_{IN+} \) is greater than the analog voltage at \( V_{IN-} \), the output of the comparator is a digital high level.

**Note:** The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

**FIGURE 8-2: COMPARATOR OUTPUT BLOCK DIAGRAM**

- Comparator output is latched on falling edge of Timer1 clock source.
- Q1 and Q3 are phases of the four-phase system clock (Fosc).
- Q1 is held high during Sleep mode.
8.2 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 8-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

**FIGURE 8-3: ANALOG INPUT MODEL**

![Analog Input Model Diagram]

**Legend:**
- CPIN = Input Capacitance
- ILEAKAGE = Leakage Current at the pin due to various junctions
- RIC = Interconnect Resistance
- RS = Source Impedance
- VA = Analog Voltage
- VT = Threshold Voltage

---

**Note 1:** When reading a PORT register, all pins configured as analog inputs will read as a ‘0’. Pins configured as digital inputs will convert as an analog input, according to the input specification.

**Note 2:** Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.
8.3 Comparator Configuration

There are eight modes of operation for the comparator. The CM<2:0> bits of the CMCON0 register are used to select these modes as shown in Figure 8-4.

- Analog function (A): digital input buffer is disabled
- Digital function (D): comparator digital output, overrides port function
- Normal port function (I/O): independent of comparator

The port pins denoted as “A” will read as a ‘0’ regardless of the state of the I/O pin or the I/O control TRIS bit. Pins used as analog inputs should also have the corresponding TRIS bit set to ‘1’ to disable the digital output driver. Pins denoted as “D” should have the corresponding TRIS bit set to ‘0’ to enable the digital output driver.

**Note:** Comparator interrupts should be disabled during a Comparator mode change to prevent unintended interrupts.

**FIGURE 8-4:** COMPARATOR I/O OPERATING MODES

<table>
<thead>
<tr>
<th>Comparator Reset (POR Default Value – low power)</th>
<th>Comparator w/o Output and with Internal Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM&lt;2:0&gt; = 000</td>
<td>CM&lt;2:0&gt; = 100</td>
</tr>
<tr>
<td>CIN-</td>
<td>A</td>
</tr>
<tr>
<td>CIN+</td>
<td>A</td>
</tr>
<tr>
<td>COUT (pin)</td>
<td>I/O</td>
</tr>
<tr>
<td>Off(1)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Comparator with Output</th>
<th>Multiplexed Input with Internal Reference and Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM&lt;2:0&gt; = 001</td>
<td>CM&lt;2:0&gt; = 101</td>
</tr>
<tr>
<td>CIN-</td>
<td>A</td>
</tr>
<tr>
<td>CIN+</td>
<td>A</td>
</tr>
<tr>
<td>COUT (pin)</td>
<td>D</td>
</tr>
<tr>
<td>COUT</td>
<td>COUT</td>
</tr>
<tr>
<td>From CVREF Module</td>
<td>From CVREF Module</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Comparator without Output</th>
<th>Multiplexed Input with Internal Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM&lt;2:0&gt; = 010</td>
<td>CM&lt;2:0&gt; = 110</td>
</tr>
<tr>
<td>CIN-</td>
<td>A</td>
</tr>
<tr>
<td>CIN+</td>
<td>A</td>
</tr>
<tr>
<td>COUT (pin)</td>
<td>I/O</td>
</tr>
<tr>
<td>COUT</td>
<td>COUT</td>
</tr>
<tr>
<td>From CVREF Module</td>
<td>From CVREF Module</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Comparator with Output and Internal Reference</th>
<th>Comparator Off (Lowest power)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM&lt;2:0&gt; = 011</td>
<td>CM&lt;2:0&gt; = 111</td>
</tr>
<tr>
<td>CIN-</td>
<td>A</td>
</tr>
<tr>
<td>CIN+</td>
<td>I/O</td>
</tr>
<tr>
<td>COUT (pin)</td>
<td>D</td>
</tr>
<tr>
<td>COUT</td>
<td>COUT</td>
</tr>
<tr>
<td>From CVREF Module</td>
<td>Off(1)</td>
</tr>
</tbody>
</table>

**Legend:**

- A = Analog Input, ports always reads ‘0’
- I/O = Normal port I/O
- CIS = Comparator Input Switch (CMCON0<3>)
- D = Comparator Digital Output

**Note 1:** Reads as ‘0’, unless CINV = 1.
8.4 Comparator Control
The CMCON0 register (Register 8-1) provides access to the following comparator features:
- Mode selection
- Output state
- Output polarity
- Input switch

8.4.1 Comparator Output State
The Comparator state can always be read internally via the COUT bit of the CMCON0 register. The comparator state may also be directed to the COUT pin in the following modes:
- \( CM<2:0> = 001 \)
- \( CM<2:0> = 011 \)
- \( CM<2:0> = 101 \)
When one of the above modes is selected, the associated TRIS bit of the COUT pin must be cleared.

8.4.2 Comparator Output Polarity
Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CINV bit of the CMCON0 register. Clearing CINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 8-1.

<table>
<thead>
<tr>
<th>Input Conditions</th>
<th>CINV</th>
<th>COUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN^+} &gt; V_{IN^-} )</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>( V_{IN^+} &lt; V_{IN^-} )</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>( V_{IN^+} &gt; V_{IN^-} )</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>( V_{IN^+} &lt; V_{IN^-} )</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Note: COUT refers to both the register bit and output pin.

8.4.3 Comparator Input Switch
The inverting input of the comparator may be switched between two analog pins in the following modes:
- \( CM<2:0> = 101 \)
- \( CM<2:0> = 110 \)
In the above modes, both pins remain in analog mode regardless of which pin is selected as the input. The CIS bit of the CMCON0 register controls the comparator input switch.

8.5 Comparator Response Time
The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in Section 15.0 “Electrical Specifications” for more details.
8.6 Comparator Interrupt Operation

The comparator interrupt flag is set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figure 8.2). One latch is updated with the comparator output level when the CMCON0 register is read. This latch retains the value until the next read of the CMCON0 register or the occurrence of a Reset. The other latch of the mismatch circuit is updated on every Q1 system clock. A mismatch condition will occur when a comparator output change is clocked through the second latch on the Q1 clock cycle. The mismatch condition will persist, holding the CMIF bit of the PIR1 register true, until either the CMCON0 register is read or the comparator output returns to the previous state.

Note: A write operation to the CMCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.

Software will need to maintain information about the status of the comparator output to determine the actual change that has occurred.

The CMIF bit of the PIR1 register, is the comparator interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit of the PIE1 register and the PEIE and GIE bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CMIF bit of the PIR1 register will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of CMCON0. This will end the mismatch condition.

b) Clear the CMIF interrupt flag.

A persistent mismatch condition will preclude clearing the CMIF interrupt flag. Reading CMCON0 will end the mismatch condition and allow the CMIF bit to be cleared.

Note: If a change in the CMCON0 register (COUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF interrupt flag may not get set.
8.7 Operation During Sleep

The comparator, if enabled before entering Sleep mode, remains active during Sleep. The additional current consumed by the comparator is shown separately in Section 15.0 “Electrical Specifications”. If the comparator is not used to wake the device, power consumption can be minimized while in Sleep mode by turning off the comparator. The comparator is turned off by selecting mode CM<2:0> = 000 or CM<2:0> = 111 of the CMCON0 register.

A change to the comparator output can wake-up the device from Sleep. To enable the comparator to wake the device from Sleep, the CMIE bit of the PIE1 register and the PEIE bit of the INTCON register must be set. The instruction following the Sleep instruction always executes following a wake from Sleep. If the GIE bit of the INTCON register is also set, the device will then execute the Interrupt Service Routine.

8.8 Effects of a Reset

A device Reset forces the CMCON0 and CMCON1 registers to their Reset states. This forces the Comparator module to be in the Comparator Reset mode (CM<2:0> = 000). Thus, all comparator inputs are analog inputs with the comparator disabled to consume the smallest current possible.

REGISTER 8-1: CMCON0: COMPARATOR CONFIGURATION REGISTER

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unimplemented</td>
<td>COUT: Comparator Output bit</td>
<td>Unimplemented</td>
<td>CINV: Comparator Output Inversion bit</td>
<td>CIS: Comparator Input Switch bit</td>
<td>CM&lt;2:0&gt;: Comparator Mode bits</td>
</tr>
<tr>
<td>R = Readable bit</td>
<td>W = Writable bit</td>
<td>U = Unimplemented bit, read as ‘0’</td>
<td>‘1’ = Bit is set</td>
<td>‘0’ = Bit is cleared</td>
<td>x = Bit is unknown</td>
</tr>
</tbody>
</table>

Legend:

- 1 = VIN+ > VIN-
- 0 = VIN+ < VIN-
- 1 = Output inverted
- 0 = Output not inverted
- CIN+ connects to VIN-
- CIN- connects to VIN-
- CIS has no effect.

- 000 = CM<2:0> = 000
- 001 = CM<2:0> = 001
- 010 = CM<2:0> = 010
- 011 = CM<2:0> = 011
- 100 = CM<2:0> = 100
- 101 = CM<2:0> = 101
- 110 = CM<2:0> = 110
- 111 = CM<2:0> = 111

000 = CIN+ connects to VIN-
001 = CIN- connects to VIN-
010 = CIN+ connects to CIN-
011 = CIN- connects to CIN+
100 = CIN+ connects to CIN-
101 = CIN- connects to CIN+
110 = CIN+ connects to CIN-
111 = CIN- connects to CIN+
8.9 Comparator Gating Timer1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CMCON1 register will enable Timer1 to increment based on the output of the comparator. This requires that Timer1 is on and gating is enabled. See Section 6.0 “Timer1 Module with Gate Control” for details.

It is recommended to synchronize the comparator with Timer1 by setting the CMSYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

8.10 Synchronizing Comparator Output to Timer1

The comparator output can be synchronized with Timer1 by setting the CMSYNC bit of the CMCON1 register. When enabled, the comparator output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 8-2) and the Timer1 Block Diagram (Figure 6-1) for more information.

REGISTER 8-2: CMCON1: COMPARATOR CONFIGURATION REGISTER

| bit 7-2 Unimplemented: Read as ‘0’ |
| bit 1 T1GSS: Timer1 Gate Source Select bit\(^{(1)}\) |
| bit 0 CMSYNC: Comparator Output Synchronization bit\(^{(2)}\) |

Legend:
- \(R\) = Readable bit
- \(W\) = Writable bit
- \(U\) = Unimplemented bit, read as ‘0’
- \(-n\) = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \(x\) = Bit is unknown

Note 1: Refer to Section 6.6 “Timer1 Gate”.
Note 2: Refer to Figure 8-2.
8.11 Comparator Voltage Reference
The Comparator Voltage Reference module provides an internally generated voltage reference for the comparators. The following features are available:

- Independent from Comparator operation
- Two 16-level voltage ranges
- Output clamped to VSS
- Ratiometric with VDD

The VRCON register (Register 8-3) controls the Voltage Reference module shown in Figure 8-7.

8.11.1 INDEPENDENT OPERATION
The comparator voltage reference is independent of the comparator configuration. Setting the VREN bit of the VRCON register will enable the voltage reference.

8.11.2 OUTPUT VOLTAGE SELECTION
The CVREF voltage reference has 2 ranges with 16 voltage levels in each range. Range selection is controlled by the VRR bit of the VRCON register. The 16 levels are set with the VR<3:0> bits of the VRCON register.

The CVREF output voltage is determined by the following equations:

EQUATION 8-1: CVREF OUTPUT VOLTAGE

\[
\begin{align*}
V_{RR} &= 1 \text{ (low range):} \\
CVREF &= (VR<3:0>/24) \times VDD \\
V_{RR} &= 0 \text{ (high range):} \\
CVREF &= (VDD/4) + (VR<3:0>/32) \times VDD
\end{align*}
\]

The full range of VSS to VDD cannot be realized due to the construction of the module. See Figure 8-1.

8.11.3 OUTPUT CLAMPED TO VSS
The CVREF output voltage can be set to Vss with no power consumption by configuring VRCON as follows:

- VREN = 0
- VRR = 1
- VR<3:0> = 0000

This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.

8.11.4 OUTPUT RATIOMETRIC TO VDD
The comparator voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in Section 15.0 “Electrical Specifications”.

REGISTER 8-3: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>VREN</td>
<td>—</td>
<td>VRR</td>
<td>—</td>
<td>VR3</td>
<td>VR2</td>
<td>VR1</td>
<td>VR0</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

- bit 7 VREN: CVREF Enable bit
  - 1 = CVREF circuit powered on
  - 0 = CVREF circuit powered down, no IDD drain and CVREF = VSS.

- bit 6 Unimplemented: Read as ‘0’

- bit 5 VRR: CVREF Range Selection bit
  - 1 = Low range
  - 0 = High range

- bit 4 Unimplemented: Read as ‘0’

- bit 3-0 VR<3:0>: CVREF Value Selection 0 ≤ VR<3:0> ≤ 15
  - When VRR = 1: CVREF = (VR<3:0>/24) \times VDD
  - When VRR = 0: CVREF = VDD/4 + (VR<3:0>/32) \times VDD
FIGURE 8-7: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

TABLE 8-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSEL</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>CMCON0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>CMCON1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>CCP1IE</td>
<td>—</td>
<td>CMIE</td>
<td>OSFIE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>00-</td>
<td>0000</td>
</tr>
<tr>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>CCP1IF</td>
<td>—</td>
<td>CMIF</td>
<td>OSFIF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>00-</td>
<td>0000</td>
</tr>
<tr>
<td>GPIO</td>
<td>—</td>
<td>—</td>
<td>GP5</td>
<td>GP4</td>
<td>GP3</td>
<td>GP2</td>
<td>GP1</td>
<td>GP0</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>TRISIO</td>
<td>—</td>
<td>—</td>
<td>TRISIO5</td>
<td>TRISIO4</td>
<td>TRISIO3</td>
<td>TRISIO2</td>
<td>TRISIO1</td>
<td>TRISIO0</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>VRCON</td>
<td>VREN</td>
<td>VRR</td>
<td>—</td>
<td>—</td>
<td>VR3</td>
<td>VR2</td>
<td>VR1</td>
<td>VR0</td>
<td>0-0-</td>
<td>0-0-0</td>
</tr>
</tbody>
</table>

Legend:  
- unknown, 0 = unchanged, - = unimplemented, read as ‘0’. Shaded cells are not used for comparator.  

Note 1: Care should be taken to ensure VREF remains within the comparator Common mode input range. See Section 15.0 “Electrical Specifications” for more detail.
9.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).

The ADC voltage reference is software selectable to either \( V_{DD} \) or a voltage applied to the external reference pins.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

Figure 9-1 shows the block diagram of the ADC.

9.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- GPIO configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

9.1.1 GPIO CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. See the corresponding GPIO section for more information.

**Note:** Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

9.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to Section 9.2 “ADC Operation” for more information.
9.1.3 ADC VOLTAGE REFERENCE
The VCFG bit of the ADCON0 register provides control of the positive voltage reference. The positive voltage reference can be either VDD or an external voltage source. The negative voltage reference is always connected to the ground reference.

9.1.4 CONVERSION CLOCK
The source of the conversion clock is software selectable via the ADCS bits of the ANSEL register. There are seven possible clock options:
- FOSC/2
- FOSC/4
- FOSC/8
- FOSC/16
- FOSC/32
- FOSC/64
- FRC (dedicated internal oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11 TAD periods as shown in Figure 9-2.

For correct conversion, the appropriate TAD specification must be met. See A/D conversion requirements in Section 15.0 “Electrical Specifications” for more information. Table 9-1 gives examples of appropriate ADC clock selections.

Note: Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

<table>
<thead>
<tr>
<th>ADC Clock Source</th>
<th>Device Frequency (Fosc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 MHz</td>
<td>8 MHz</td>
</tr>
<tr>
<td>FOSC/2</td>
<td>100 ns(^{(2)})</td>
</tr>
<tr>
<td>FOSC/4</td>
<td>200 ns(^{(2)})</td>
</tr>
<tr>
<td>FOSC/8</td>
<td>400 ns(^{(2)})</td>
</tr>
<tr>
<td>FOSC/16</td>
<td>800 ns(^{(2)})</td>
</tr>
<tr>
<td>FOSC/32</td>
<td>1.6 (\mu s)</td>
</tr>
<tr>
<td>FOSC/64</td>
<td>3.2 (\mu s)</td>
</tr>
<tr>
<td>FRC</td>
<td>2.6 (\mu s(^{(1,4)})</td>
</tr>
</tbody>
</table>

Legend: Shaded cells are outside of recommended range.

Note 1: The FRC source has a typical TAD time of 4 \(\mu s\) for VDD > 3.0V.
2: These values violate the minimum required TAD time.
3: For faster conversion times, the selection of another clock source is recommended.
4: When the device frequency is greater than 1 MHz, the FRC clock source is only recommended if the conversion will be performed during Sleep.

FIGURE 9-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES

TCY to TAD1 TAD2 TAD3 TAD4 TAD5 TAD6 TAD7 TAD8 TAD9 TAD10 TAD11
Conversion Starts
Holding Capacitor is Disconnected from Analog Input (typically 100 ns)
Set GO/DONE bit
ADRESH and ADRESL registers are loaded,
GO bit is cleared,
ADIF bit is set,
Holding capacitor is connected to analog input
9.1.5 INTERRUPTS
The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC interrupt flag is the ADIF bit in the PIR1 register. The ADC interrupt enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note: The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the global interrupt must be disabled. If the global interrupt is enabled, execution will switch to the interrupt service routine.

Please see Section 12.4 “Interrupts” for more information.

FIGURE 9-3: 10-BIT A/D CONVERSION RESULT FORMAT

9.1.6 RESULT FORMATTING
The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON0 register controls the output format. Figure 9-3 shows the two output formats.

9.2 ADC Operation

9.2.1 STARTING A CONVERSION
To enable the ADC module, the ADON bit of the ADCON0 register must be set to a ‘1’. Setting the GO/DONE bit of the ADCON0 register to a ‘1’ will start the Analog-to-Digital conversion.

Note: The GO/DONE bit should not be set in the same instruction that turns on the ADC. Refer to Section 9.2.6 “A/D Conversion Procedure”.

9.2.2 COMPLETION OF A CONVERSION
When the conversion is complete, the ADC module will:
- Clear the GO/DONE bit
- Set the ADIF flag bit
- Update the ADRESH:ADRESL registers with new conversion result

9.2.3 TERMINATING A CONVERSION
If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete Analog-to-Digital conversion sample. Instead, the ADRESH:ADRESL register pair will retain the value of the previous conversion. Additionally, a 2 TAD delay is required before another acquisition can be initiated. Following this delay, an input acquisition is automatically started on the selected channel.

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.
9.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

9.2.5 SPECIAL EVENT TRIGGER

The CCP Special Event Trigger allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/DONE bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not assure proper ADC timing. It is the user’s responsibility to ensure that the ADC timing requirements are met.

See Section 11.0 “Capture/Compare/PWM (CCP) Module” for more information.

9.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure GPIO Port:
   • Disable pin output driver (See TRIS register)
   • Configure pin as analog
2. Configure the ADC module:
   • Select ADC conversion clock
   • Configure voltage reference
   • Select ADC input channel
   • Select result format
   • Turn on ADC module
3. Configure ADC interrupt (optional):
   • Clear ADC interrupt flag
   • Enable ADC interrupt
   • Enable peripheral interrupt
   • Enable global interrupt(1)
4. Wait the required acquisition time(2).
5. Start conversion by setting the GO/DONE bit.
6. Wait for ADC conversion to complete by one of the following:
   • Polling the GO/DONE bit
   • Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

Note 2: See Section 9.3 “A/D Acquisition Requirements”.

EXAMPLE 9-1: A/D CONVERSION

;This code block configures the ADC
;for polling, Vdd reference, Frc clock
;and GP0 input.
;
;Conversion start & polling for completion
;are included.
;
BANKSEL TRISIO ;
BSF TRISIO,0 ;Set GP0 to input
BANKSEL ANSEL ;
MOVLW B’01110001’ ;ADC Frc clock,
IORWF ANSEL ; and GP0 as analog
BANKSEL ADCON0 ;
MOVLW B’10000001’ ;Right justify,
MOVWF ADCON0 ;Vdd Vref, AN0, On
CALL SampleTime ;Acquisition delay
BSF ADCON0,GO ;Start conversion
BTFSC ADCON0,GO ;Is conversion done?
GOTO $-1 ;No, test again
BANKSEL ADRESH ;
MOVF ADRESH,W ;Read upper 2 bits
MOVWF RESULTHI ;Store in GPR space
BANKSEL ADRESL ;
MOVF ADRESL,W ;Read lower 8 bits
MOVWF RESULTLO ;Store in GPR space

9.2.7 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.
### REGISTER 9-1: ADCON0: A/D CONTROL REGISTER 0

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>ADON</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADFM</td>
<td>VCFG</td>
<td>—</td>
<td>—</td>
<td>CHS1</td>
<td>CHS0</td>
<td>GO/DONE</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ADFM</strong>: A/D Conversion Result Format Select bit</td>
<td></td>
</tr>
<tr>
<td>1 = Right justified</td>
<td>0 = Left justified</td>
</tr>
<tr>
<td><strong>VCFG</strong>: Voltage Reference bit</td>
<td></td>
</tr>
<tr>
<td>1 = VREF pin</td>
<td>0 = VDD</td>
</tr>
<tr>
<td><strong>CHS&lt;1:0&gt;</strong>: Analog Channel Select bits</td>
<td></td>
</tr>
<tr>
<td>00 = AN0</td>
<td>01 = AN1</td>
</tr>
<tr>
<td>10 = AN2</td>
<td>11 = AN3</td>
</tr>
<tr>
<td><strong>GO/DONE</strong>: A/D Conversion Status bit</td>
<td></td>
</tr>
<tr>
<td>1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle. This bit is automatically cleared by hardware when the A/D conversion has completed.</td>
<td></td>
</tr>
<tr>
<td>0 = A/D conversion completed/not in progress</td>
<td></td>
</tr>
<tr>
<td><strong>ADON</strong>: ADC Enable bit</td>
<td></td>
</tr>
<tr>
<td>1 = ADC is enabled</td>
<td>0 = ADC is disabled and consumes no operating current</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown
REGISTER 9-2: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ADRESH&lt;9&gt;</td>
</tr>
<tr>
<td>6</td>
<td>ADRESH&lt;8&gt;</td>
</tr>
<tr>
<td>5</td>
<td>ADRESH&lt;7&gt;</td>
</tr>
<tr>
<td>4</td>
<td>ADRESH&lt;6&gt;</td>
</tr>
<tr>
<td>3</td>
<td>ADRESH&lt;5&gt;</td>
</tr>
<tr>
<td>2</td>
<td>ADRESH&lt;4&gt;</td>
</tr>
<tr>
<td>1</td>
<td>ADRESH&lt;3&gt;</td>
</tr>
<tr>
<td>0</td>
<td>ADRESH&lt;2&gt;</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- 
- **-n** = Value at POR
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **x** = Bit is unknown

bit 7-0  ADRESH<9:2>: ADC Result Register bits
Upper 8 bits of 10-bit conversion result

REGISTER 9-3: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ADRESL&lt;7&gt;</td>
</tr>
<tr>
<td>6</td>
<td>ADRESL&lt;6&gt;</td>
</tr>
<tr>
<td>5</td>
<td>ADRESL&lt;5&gt;</td>
</tr>
<tr>
<td>4</td>
<td>ADRESL&lt;4&gt;</td>
</tr>
<tr>
<td>3</td>
<td>ADRESL&lt;3&gt;</td>
</tr>
<tr>
<td>2</td>
<td>ADRESL&lt;2&gt;</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- 
- **-n** = Value at POR
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **x** = Bit is unknown

bit 7-0  ADRESL<7:0>: ADC Result Register bits
Lower 2 bits of 10-bit conversion result

REGISTER 9-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ADRESH&lt;9&gt;</td>
</tr>
<tr>
<td>6</td>
<td>ADRESH&lt;8&gt;</td>
</tr>
<tr>
<td>5</td>
<td>ADRESH&lt;7&gt;</td>
</tr>
<tr>
<td>4</td>
<td>ADRESH&lt;6&gt;</td>
</tr>
<tr>
<td>3</td>
<td>ADRESH&lt;5&gt;</td>
</tr>
<tr>
<td>2</td>
<td>ADRESH&lt;4&gt;</td>
</tr>
<tr>
<td>1</td>
<td>ADRESH&lt;3&gt;</td>
</tr>
<tr>
<td>0</td>
<td>ADRESH&lt;2&gt;</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- 
- **-n** = Value at POR
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **x** = Bit is unknown

bit 7-2  Reserved: Do not use.

REGISTER 9-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ADRESL&lt;7&gt;</td>
</tr>
<tr>
<td>6</td>
<td>ADRESL&lt;6&gt;</td>
</tr>
<tr>
<td>5</td>
<td>ADRESL&lt;5&gt;</td>
</tr>
<tr>
<td>4</td>
<td>ADRESL&lt;4&gt;</td>
</tr>
<tr>
<td>3</td>
<td>ADRESL&lt;3&gt;</td>
</tr>
<tr>
<td>2</td>
<td>ADRESL&lt;2&gt;</td>
</tr>
<tr>
<td>1</td>
<td>ADRESL&lt;1&gt;</td>
</tr>
<tr>
<td>0</td>
<td>ADRESL&lt;0&gt;</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- 
- **-n** = Value at POR
- **’1’** = Bit is set
- **’0’** = Bit is cleared
- **x** = Bit is unknown

bit 7-0  ADRESL<7:0>: ADC Result Register bits
Lower 8 bits of 10-bit conversion result
9.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (C HOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 9-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (V DD), see Figure 9-4. The maximum recommended impedance for analog sources is 10 kΩ. As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 9-1 may be used. This equation assumes that 1/2 LSB error is used (1024 steps for the ADC). The 1/2 LSB error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 9-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10kΩ 5.0V VDD

\[ T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \]
\[ = T_{AMP} + T_{C} + T_{COFF} \]
\[ = 2\mu s + T_{C} + ([\text{Temperature} - 25^\circ\text{C}])(0.05\mu s/\circ\text{C}) \]

The value for TC can be approximated with the following equations:

\[ V_{APPLIED}\left(1 - \frac{1}{2047}\right) = V_{CHOLD} \quad ;[1] \text{VCHOLD charged to within 1/2 lsb} \]
\[ V_{APPLIED}\left(1 - e^{-\frac{T_{C}}{RC}}\right) = V_{CHOLD} \quad ;[2] \text{VCHOLD charge response to VAPPLIED} \]
\[ V_{APPLIED}\left(1 - e^{-\frac{T_{C}}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{2047}\right) \quad ;\text{combining [1] and [2]} \]

Solving for TC:

\[ T_{C} = -C_{HOLD}(R_{IC} + R_{SS} + R_{S}) \ln(1/2047) \]
\[ = -10\mu F(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.0004885) \]
\[ = 1.37\mu s \]

Therefore:

\[ T_{ACQ} = 2\mu s + 1.37\mu s + [(50^\circ\text{C} - 25^\circ\text{C})(0.05\mu s/\circ\text{C})] \]
\[ = 4.67\mu s \]

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (C HOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.
FIGURE 9-4: ANALOG INPUT MODEL

Legend:  
CPIN = Input Capacitance  
VT = Threshold Voltage  
I LEAKAGE = Leakage current at the pin due to various junctions  
RIC = Interconnect Resistance  
SS = Sampling Switch  
CHOLD = Sample/Hold Capacitance

FIGURE 9-5: ADC TRANSFER FUNCTION

ADC Output Code

<table>
<thead>
<tr>
<th>3FFh</th>
<th>3FEh</th>
<th>3FDh</th>
<th>3FCh</th>
<th>3FBh</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-Scale Range</td>
<td>1 LSB ideal</td>
<td>Full-Scale Transition</td>
<td>Analog Input Voltage</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>004h</th>
<th>003h</th>
<th>002h</th>
<th>001h</th>
<th>000h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero-Scale Transition</td>
<td>1 LSB ideal</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
TABLE 9-2: SUMMARY OF ASSOCIATED ADC REGISTERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCON0</td>
<td>ADFM</td>
<td>VCFG</td>
<td>—</td>
<td>—</td>
<td>CHS1</td>
<td>CHS0</td>
<td>GO/DONE</td>
<td>ADON</td>
<td>00-- 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>ANSEL</td>
<td>—</td>
<td>ADCS2</td>
<td>ADCS1</td>
<td>ADCS0</td>
<td>ANS3</td>
<td>ANS2</td>
<td>ANS1</td>
<td>ANS0</td>
<td>-000 1111</td>
<td>-000 1111</td>
</tr>
<tr>
<td>ADRESH</td>
<td>A/D Result Register High Byte</td>
<td>xxxxx</td>
<td>xxxx</td>
<td>xxxx</td>
<td>uuuu</td>
<td>uuuu</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADRESL</td>
<td>A/D Result Register Low Byte</td>
<td>xxxxx</td>
<td>xxxx</td>
<td>xxxx</td>
<td>uuuu</td>
<td>uuuu</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>CCP1IE</td>
<td>—</td>
<td>CMIE</td>
<td>OSFIE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>000- 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>CCP1IF</td>
<td>—</td>
<td>CMIF</td>
<td>OSFIF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>000- 0000</td>
<td>000- 0000</td>
</tr>
<tr>
<td>GPIO</td>
<td>—</td>
<td>—</td>
<td>GP5</td>
<td>GP4</td>
<td>GP3</td>
<td>GP2</td>
<td>GP1</td>
<td>GP0</td>
<td>--xx xxxx</td>
<td>--uu uuuu</td>
</tr>
<tr>
<td>TRISIO</td>
<td>—</td>
<td>—</td>
<td>TRISIO5</td>
<td>TRISIO4</td>
<td>TRISIO3</td>
<td>TRISIO2</td>
<td>TRISIO1</td>
<td>TRISIO0</td>
<td>--11 1111</td>
<td>--11 1111</td>
</tr>
</tbody>
</table>

Legend:  
- x = unknown, u = unchanged, — = unimplemented read as “0”. Shaded cells are not used for ADC module.
10.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory:

- EECON1
- EECON2 (not a physically implemented register)
- EEDAT
- EEADR

EEDAT holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC12F683 has 256 bytes of data EEPROM with an address range from 0h to FFh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature as well as from chip-to-chip. Please refer to AC Specifications in Section 15.0 “Electrical Specifications” for exact limits.

When the data memory is code-protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access the data EEPROM data and will read zeroes.

REGISTER 10-1: EEDAT: EEPROM DATA REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEDAT7</td>
<td>EEDAT6</td>
<td>EEDAT5</td>
<td>EEDAT4</td>
<td>EEDAT3</td>
<td>EEDAT2</td>
<td>EEDAT1</td>
<td>EEDAT0</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
  - '1' = Bit is set
  - '0' = Bit is cleared
  - x = Bit is unknown

bit 7-0  EEDATn: Byte Value to Write To or Read From Data EEPROM bits

REGISTER 10-2: EEADR: EEPROM ADDRESS REGISTER

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEADR7</td>
<td>EEADR6</td>
<td>EEADR5</td>
<td>EEADR4</td>
<td>EEADR3</td>
<td>EEADR2</td>
<td>EEADR1</td>
<td>EEADR0</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
  - '1' = Bit is set
  - '0' = Bit is cleared
  - x = Bit is unknown

bit 7-0  EEADR: Specifies One of 256 Locations for EEPROM Read/Write Operation bits
10.1 EECON1 and EECON2 Registers

EECON1 is the control register with four low-order bits physically implemented. The upper four bits are non-implemented and read as ‘0’ s.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR Reset, or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit, clear it and rewrite the location. The data and address will be cleared. Therefore, the EEDAT and EEADR registers will need to be re-initialized.

Interrupt flag, EEIF bit of the PIR1 register, is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all ‘0’ s. The EECON2 register is used exclusively in the data EEPROM write sequence.

REGISTER 10-3: EECON1: EEPROM CONTROL REGISTER

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-x</th>
<th>R/W-0</th>
<th>R/S-0</th>
<th>R/S-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>WRERR</td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
</tr>
</tbody>
</table>

| bit 7-4 | Unimplemented: Read as ‘0’ |
| bit 3   | WRERR: EEPROM Error Flag bit |
|        | 1 = A write operation is prematurely terminated (any MCLR Reset, any WDT Reset during normal operation or BOR Reset) |
|        | 0 = The write operation completed |

| bit 2   | WREN: EEPROM Write Enable bit |
|        | 1 = Allows write cycles |
|        | 0 = Inhibits write to the data EEPROM |

| bit 1   | WR: Write Control bit |
|        | 1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.) |
|        | 0 = Write cycle to the data EEPROM is complete |

| bit 0   | RD: Read Control bit |
|        | 1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.) |
|        | 0 = Does not initiate an EEPROM read |

Legend:

S = Bit can only be set
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-\text{-n} = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
\text{x} = Bit is unknown
10.2 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD of the EECON1 register, as shown in Example 10-1. The data is available, at the very next cycle, in the EEDAT register. Therefore, it can be read in the next instruction. EEDAT holds this value until another read, or until it is written to by the user (during a write operation).

**EXAMPLE 10-1: DATA EEPROM READ**

```
BANKSEL EEADR;
MOVLW CONFIG_ADDR;
MOVWF EEADR ;Address to read
BSF EECON1,RD ;EE Read
MOVF EEDAT,W
```

10.3 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDAT register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 10-2.

**EXAMPLE 10-2: DATA EEPROM WRITE**

```
BANKSEL EECON1;
BSF EECON1,WREN ;Enable write
BCF INTCON,GIE ;Disable INTs
BTFSC INTCON,GIE ;See AN576
GOTO $-2 ;
MOVLW 55h ;Unlock write
MOVWF EECON2 ;
MOVLW AAh ;
MOVWF EECON2 ;
BSF EECON1,WR ;Start the write
BSF INTCON,GIE ;Enable INTs
```

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit of the PIR1 register must be cleared by software.

10.4 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM should be verified (see Example 10-3) to the desired value to be written.

**EXAMPLE 10-3: WRITE VERIFY**

```
BANKSEL EEDAT;
MOVF EEDAT,W ;EEDAT not changed from previous write
BSF EECON1,RD ;YES, Read the value written
XORWF EEDAT,W
BTFSS STATUS,Z ;Is data the same
GOTO WRITE_ERR ;No, handle error
: ;Yes, continue
```

10.4.1 USING THE DATA EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). When variables in one section change frequently, while variables in another section do not change, it is possible to exceed the total number of write cycles to the EEPROM (specification D124) without exceeding the total number of write cycles to a single byte (specifications D120 and D120A). If this is the case, then a refresh of the array must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.
10.5 Protection Against Spurious Write

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (64 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:
- Brown-out
- Power Glitch
- Software Malfunction

10.6 Data EEPROM Operation During Code-Protect

Data memory can be code-protected by programming the CPD bit in the Configuration Word register (Register 12-1) to ‘0’.

When the data memory is code-protected, the CPU is able to read and write data to the data EEPROM. It is recommended to code-protect the program memory when code-protecting data memory. This prevents anyone from programming zeroes over the existing code (which will execute as _NOPs_) to reach an added routine, programmed in unused program memory, which outputs the contents of data memory. Programming unused locations in program memory to ‘0’ will also help prevent data memory code protection from becoming breached.

### TABLE 10-1: SUMMARY OF ASSOCIATED DATA EEPROM REGISTERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>CCP1IF</td>
<td>CMIF</td>
<td>OSFIF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>0000-0000 0000-0000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>CCP1IE</td>
<td>CMIE</td>
<td>OSPIE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>0000-0000 0000-0000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EEDAT</td>
<td>EEDAT7</td>
<td>EEDAT6</td>
<td>EEDAT5</td>
<td>EEDAT4</td>
<td>EEDAT3</td>
<td>EEDAT2</td>
<td>EEDAT1</td>
<td>EEDAT0</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>EEADR</td>
<td>EEADR7</td>
<td>EEADR6</td>
<td>EEADR5</td>
<td>EEADR4</td>
<td>EEADR3</td>
<td>EEADR2</td>
<td>EEADR1</td>
<td>EEADR0</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>EECON1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WRERR</td>
<td>WREN</td>
<td>WR</td>
<td>RD</td>
</tr>
<tr>
<td>EECON2(1)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Legend:**
x = unknown, u = unchanged, – = unimplemented read as ‘0’, q = value depends upon condition. Shaded cells are not used by the Data EEPROM module.

**Note 1:** EECON2 is not a physical register.
11.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate a Pulse-Width Modulated signal of varying frequency and duty cycle.

The timer resources used by the module are shown in Table 11-1.

Additional information on CCP modules is available in the Application Note AN594, “Using the CCP Modules” (DS00594).

**TABLE 11-1: CCP MODE – TIMER RESOURCES REQUIRED**

<table>
<thead>
<tr>
<th>CCP Mode</th>
<th>Timer Resource</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capture</td>
<td>Timer1</td>
</tr>
<tr>
<td>Compare</td>
<td>Timer1</td>
</tr>
<tr>
<td>PWM</td>
<td>Timer2</td>
</tr>
</tbody>
</table>

**REGISTER 11-1: CCP1CON: CCP1 CONTROL REGISTER**

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>DC1B1</td>
<td>DC1B0</td>
<td>CCP1M3</td>
<td>CCP1M2</td>
<td>CCP1M1</td>
<td>CCP1M0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Legend:</th>
</tr>
</thead>
<tbody>
<tr>
<td>R = Readable bit</td>
</tr>
<tr>
<td>-n = Value at POR</td>
</tr>
</tbody>
</table>

| bit 7-6 | Unimplemented: Read as ‘0’ |
| bit 5-4 | DC1B<1:0>: PWM Duty Cycle Least Significant bits |
|        | Capture mode: |
|        | Unused. |
|        | Compare mode: |
|        | Unused. |
|        | PWM mode: |
|        | These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L. |

| bit 3-0 | CCP1M<3:0>: CCP Mode Select bits |
|        | 0000 = Capture/Compare/PWM off (resets CCP module) |
|        | 0001 = Unused (reserved) |
|        | 0010 = Unused (reserved) |
|        | 0011 = Unused (reserved) |
|        | 0100 = Capture mode, every falling edge |
|        | 0101 = Capture mode, every rising edge |
|        | 0110 = Capture mode, every 4th rising edge |
|        | 0111 = Capture mode, every 16th rising edge |
|        | 1000 = Compare mode, set output on match (CCP1IF bit is set) |
|        | 1001 = Compare mode, clear output on match (CCP1IF bit is set) |
|        | 1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected) |
|        | 1011 = Compare mode, trigger special event (CCP1IF bit is set. TMR1 is reset and A/D conversion is started if the ADC module is enabled. CCP1 pin is unaffected.) |
|        | 110x = PWM mode active-high |
|        | 111x = PWM mode active-low |
11.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR1 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPR1H, CCPR1L register pair is read, the old captured value is overwritten by the new captured value (see Figure 11-1).

11.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the associated TRIS control bit.

**Note:** If the CCP1 pin is configured as an output, a write to the GPIO port can cause a capture condition.

11.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

11.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit of the PIE1 register clear to avoid false interrupts. Additionally, the user should clear the CCP1IF interrupt flag bit of the PIR1 register following any change in operating mode.

11.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCP1M<3:0> bits of the CCP1CON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCP1CON register before changing the prescaler (see Example 11-1).

**EXAMPLE 11-1: CHANGING BETWEEN CAPTURE PRESCALERS**

```plaintext
BANKSEL CCP1CON ;Set Bank bits to point to CCP1CON
CLR CCP1CON ;Turn CCP module off
MOVLW NEW_CAPT_PS ;Load the W reg with the new prescaler
MOVWF CCP1CON ;move value and CCP ON
MOVWF CCP1CON ;Load CCP1CON with this value
```

**FIGURE 11-1: CAPTURE MODE OPERATION BLOCK DIAGRAM**

- Set Flag bit CCP1IF (PIR1 register)
- Prescaler = 1, 4, 16
- CCP1 pin
- and Edge Detect
- Capture Enable
- TMR1H, TMR1L
- System Clock (Fosc)

**Note:** If the CCP1 pin is configured as an output, a write to the GPIO port can cause a capture condition.
11.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 module may:

- Toggle the CCP1 output.
- Set the CCP1 output.
- Clear the CCP1 output.
- Generate a Special Event Trigger.
- Generate a Software Interrupt.

The action on the pin is based on the value of the CCP1M<3:0> control bits of the CCP1CON register. All Compare modes can generate an interrupt.

FIGURE 11-2: COMPARE MODE OPERATION BLOCK DIAGRAM

11.2.1 CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the associated TRIS bit.

Note: Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the GPIO I/O data latch.

11.2.2 TIMER1 MODE SELECTION

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

11.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCP1M<3:0> = 1010), the CCP1 module does not assert control of the CCP1 pin (see the CCP1CON register).

11.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCP1M<3:0> = 1011), the CCP1 module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled

The CCP1 module does not assert control of the CCP1 pin in this mode (see the CCP1CON register).

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPR1H, CCPR1L register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. This allows the CCPR1H, CCPR1L register pair to effectively provide a 16-bit programmable period register for Timer1.

Note 1: The Special Event Trigger from the CCP module does not set interrupt flag bit TMRxIF of the PIR1 register.

2: Removing the match condition by changing the contents of the CCPR1H and CCPR1L register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.
11.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCP1 pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPR1L
- CCP1CON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCP1 pin. Since the CCP1 pin is multiplexed with the PORT data latch, the TRIS for that pin must be cleared to enable the CCP1 pin output driver.

**Note:** Clearing the CCP1CON register will relinquish CCP1 control of the CCP1 pin.

The PWM output (Figure 11-4) has a time base (period) and a time that the output stays high (duty cycle).

**FIGURE 11-4: CCP PWM OUTPUT**

<table>
<thead>
<tr>
<th>Period</th>
<th>Pulse Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMR2 = PR2</td>
<td>TMR2 = CCPR1L:CCP1CON&lt;5:4&gt;</td>
</tr>
<tr>
<td>TMR2 = 0</td>
<td></td>
</tr>
</tbody>
</table>

Figure 11-1 shows a simplified block diagram of PWM operation.

Figure 11-4 shows a typical waveform of the PWM signal.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see Section 11.3.7 “Setup for PWM Operation”.

**FIGURE 11-3: SIMPLIFIED PWM BLOCK DIAGRAM**

- **CCPR1L**
- **CCP1CON<5:4>**
- **CCPR1H(Slave)**
- **Comparator**
- **TMR2**
- **PR2**

**Note 1:** The 8-bit timer TMR2 register is concatenated with the 2-bit internal system clock (Fosc), or 2 bits of the prescaler, to create the 10-bit time base.

**Note 2:** In PWM mode, CCPR1H is a read-only register.
11.3.1 PWM PERIOD
The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 11-1.

**EQUATION 11-1: PWM PERIOD**

\[
\text{PWM Period} = \frac{(PR2 + 1) \cdot 4 \cdot T_{osc}}{(\text{TMR2 Prescale Value})}
\]

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPR1L into CCPR1H.

**Note:** The Timer2 postscaler (see Section 7.0 “Timer2 Module”) is not used in the determination of the PWM frequency.

11.3.2 PWM DUTY CYCLE
The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPR1L register and DC1B<1:0> bits of the CCP1CON register. The CCPR1L register contains the eight MSbs and the CCP1<1:0> bits of the CCP1CON register contain the two LSbs. CCPR1L and DC1B<1:0> bits of the CCP1CON register can be written to at any time. The duty cycle value is not latched into CCPR1H until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPR1H register is read-only.

Equation 11-2 is used to calculate the PWM pulse width.

Equation 11-3 is used to calculate the PWM duty cycle ratio.

11.3.3 PWM RESOLUTION
The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 11-4.

**EQUATION 11-2: PULSE WIDTH**

\[
Pulse \text{ Width} = (\text{CCPR1L:CCP1CON}<5:4>) \cdot T_{osc} \cdot \text{TMR2 Prescale Value}
\]

**EQUATION 11-3: DUTY CYCLE RATIO**

\[
\text{Duty Cycle Ratio} = \frac{(\text{CCPR1L:CCP1CON}<5:4>)}{4(PR2 + 1)}
\]

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (Fosc), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPR1H and 2-bit latch, then the CCP1 pin is cleared (see Figure 11-1).

**TABLE 11-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)**

<table>
<thead>
<tr>
<th>PWM Frequency</th>
<th>1.22 kHz</th>
<th>4.88 kHz</th>
<th>19.53 kHz</th>
<th>78.12 kHz</th>
<th>156.3 kHz</th>
<th>208.3 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer Prescale (1, 4, 16)</td>
<td>16</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>PR2 Value</td>
<td>0xFF</td>
<td>0xFF</td>
<td>0xFF</td>
<td>0x3F</td>
<td>0x1F</td>
<td>0x17</td>
</tr>
<tr>
<td>Maximum Resolution (bits)</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>8</td>
<td>7</td>
<td>6.6</td>
</tr>
</tbody>
</table>

**TABLE 11-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)**

<table>
<thead>
<tr>
<th>PWM Frequency</th>
<th>1.22 kHz</th>
<th>4.90 kHz</th>
<th>19.61 kHz</th>
<th>76.92 kHz</th>
<th>153.85 kHz</th>
<th>200.0 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer Prescale (1, 4, 16)</td>
<td>16</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>PR2 Value</td>
<td>0x65</td>
<td>0x65</td>
<td>0x65</td>
<td>0x19</td>
<td>0x0C</td>
<td>0x09</td>
</tr>
<tr>
<td>Maximum Resolution (bits)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>6</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

**Note:** If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.
11.3.4 OPERATION IN SLEEP MODE
In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

11.3.5 CHANGES IN SYSTEM CLOCK FREQUENCY
The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See Section 3.0 “Oscillator Module (With Fail-Safe Clock Monitor)” for additional details.

11.3.6 EFFECTS OF RESET
Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

11.3.7 SETUP FOR PWM OPERATION
The following steps should be taken when configuring the CCP module for PWM operation:
1. Disable the PWM pin (CCP1) output drivers by setting the associated TRIS bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCP1CON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPR1L register and DC1B bits of the CCP1CON register.
5. Configure and start Timer2:
   • Clear the TMR2IF interrupt flag bit of the PIR1 register.
   • Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
   • Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
   • Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
   • Enable the CCP1 pin output driver by clearing the associated TRIS bit.
### TABLE 11-4: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE AND TIMER1

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCP1CON</td>
<td>—</td>
<td>—</td>
<td>DC1B1</td>
<td>DC1B0</td>
<td>CCP1M3</td>
<td>CCP1M2</td>
<td>CCP1M1</td>
<td>CCP1M0</td>
<td>——000000</td>
<td>——000000</td>
</tr>
<tr>
<td>CCPR1L</td>
<td>Capture/Compare/PWM Register 1 Low Byte (LSB)</td>
<td>xxxxx</td>
<td>xxxxx</td>
<td>xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMCON1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>T1GS</td>
<td>CMSYNC</td>
<td>---- --10</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0IF</td>
<td>INTE</td>
<td>QIF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>CCP1IE</td>
<td>—</td>
<td>CMIE</td>
<td>OSFIE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>000- 0000</td>
<td>000- 0000</td>
</tr>
<tr>
<td>PR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>CCP1IF</td>
<td>—</td>
<td>CMIF</td>
<td>OSFIF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>000- 0000</td>
<td>000- 0000</td>
</tr>
<tr>
<td>T1CON</td>
<td>T1GINV</td>
<td>TMR1GE</td>
<td>T1CKPS1</td>
<td>T1CKPS0</td>
<td>T1OSCEN</td>
<td>TTSYNC</td>
<td>TMR1CS</td>
<td>TMR1ON</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>TMR1L</td>
<td>Holding Register for the Least Significant Byte of the 16-bit TMR1 Register</td>
<td>xxxxx</td>
<td>xxxxx</td>
<td>xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMR1H</td>
<td>Holding Register for the Most Significant Byte of the 16-bit TMR1 Register</td>
<td>xxxxx</td>
<td>xxxxx</td>
<td>xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRISIO</td>
<td>—</td>
<td>—</td>
<td>TRISIO5</td>
<td>TRISIO4</td>
<td>TRISIO3</td>
<td>TRISIO2</td>
<td>TRISIO1</td>
<td>TRISIO0</td>
<td>--11 1111</td>
<td>--11 1111</td>
</tr>
</tbody>
</table>

**Legend:** — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture and Compare.

### TABLE 11-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCP1CON</td>
<td>—</td>
<td>—</td>
<td>DC1B1</td>
<td>DC1B0</td>
<td>CCP1M3</td>
<td>CCP1M2</td>
<td>CCP1M1</td>
<td>CCP1M0</td>
<td>——000000</td>
<td>——000000</td>
</tr>
<tr>
<td>CCPR1L</td>
<td>Capture/Compare/PWM Register 1 Low Byte (LSB)</td>
<td>xxxxx</td>
<td>xxxxx</td>
<td>xxxxx</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMCON1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>T1GS</td>
<td>CMSYNC</td>
</tr>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0IF</td>
<td>INTE</td>
<td>QIF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>CCP1IE</td>
<td>—</td>
<td>CMIE</td>
<td>OSFIE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>000- 0000</td>
<td>000- 0000</td>
</tr>
<tr>
<td>PR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>CCP1IF</td>
<td>—</td>
<td>CMIF</td>
<td>OSFIF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>000- 0000</td>
<td>000- 0000</td>
</tr>
<tr>
<td>PR2</td>
<td>Timer2 Period Register</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
<tr>
<td>T2CON</td>
<td>—</td>
<td>TOUTPS3</td>
<td>TOUTPS2</td>
<td>TOUTPS1</td>
<td>TOUTPS0</td>
<td>TMR2ON</td>
<td>T2CKPS1</td>
<td>T2CKPS0</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>TMR2</td>
<td>Timer2 Module Register</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>TRISIO</td>
<td>—</td>
<td>—</td>
<td>TRISIO5</td>
<td>TRISIO4</td>
<td>TRISIO3</td>
<td>TRISIO2</td>
<td>TRISIO1</td>
<td>TRISIO0</td>
<td>--11 1111</td>
<td>--11 1111</td>
</tr>
</tbody>
</table>

**Legend:** — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the PWM.
12.0 SPECIAL FEATURES OF THE CPU

The PIC12F683 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator Selection
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™

The PIC12F683 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer Wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options (see Register 12-1).

---

**Note:** Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See “PIC12F6XX/16F6XX Memory Programming Specification” (DS41204) for more information.

12.1 Configuration Bits

The Configuration bits can be programmed (read as ‘0’), or left unprogrammed (read as ‘1’) to select various device configurations as shown in Register 12-1. These bits are mapped in program memory location 2007h.
**REGISTER 12-1: CONFIG: CONFIGURATION WORD REGISTER**

<table>
<thead>
<tr>
<th>bit 15-8</th>
<th>FCMEN</th>
<th>IESO</th>
<th>BOREN1</th>
<th>BOREN0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7-0</td>
<td>CPD</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWRTE</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W =Writable bit
- P = Programmable
- U = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**bit 15-12**
- **Unimplemented**: Read as ‘1’

**bit 11**
- **FCMEN**: Fail-Safe Clock Monitor Enabled bit
  - 1 = Fail-Safe Clock Monitor is enabled
  - 0 = Fail-Safe Clock Monitor is disabled

**bit 10**
- **IESO**: Internal External Switchover bit
  - 1 = Internal External Switchover mode is enabled
  - 0 = Internal External Switchover mode is disabled

**bit 9-8**
- **BOREN<1:0>**: Brown-out Reset Selection bits\(^{(1)}\)
  - 11 = BOR enabled
  - 10 = BOR enabled during operation and disabled in Sleep
  - 01 = BOR controlled by SBOREN bit of the PCON register
  - 00 = BOR disabled

**bit 7**
- **CPD**: Data Code Protection bit\(^{(2)}\)
  - 1 = Data memory code protection is disabled
  - 0 = Data memory code protection is enabled

**bit 6**
- **CP**: Code Protection bit\(^{(3)}\)
  - 1 = Program memory code protection is disabled
  - 0 = Program memory code protection is enabled

**bit 5**
- **MCLRE**: GP3/MCLR pin function select bit\(^{(4)}\)
  - 1 = GP3/MCLR pin function is MCLR
  - 0 = GP3/MCLR pin function is digital input, MCLR internally tied to VDD

**bit 4**
- **PWRTE**: Power-up Timer Enable bit
  - 1 = PWRT disabled
  - 0 = PWRT enabled

**bit 3**
- **WDTE**: Watchdog Timer Enable bit
  - 1 = WDT enabled
  - 0 = WDT disabled and can be enabled by SWDTEN bit of the WDTCON register

**bit 2-0**
- **FOSC<2:0>**: Oscillator Selection bits
  - 111 = RC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
  - 110 = RCIO oscillator: I/O function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
  - 101 = INTOSC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
  - 100 = INTOSCIO oscillator: I/O function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
  - 011 = EC: I/O function on GP4/OSC2/CLKOUT pin, CLKIN on GP5/OSC1/CLKIN
  - 010 = HS oscillator: High-speed crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
  - 001 = XT oscillator: Crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
  - 000 = LP oscillator: Low-power crystal on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN

**Note**
1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire data EEPROM will be erased when the code protection is turned off.
3: The entire program memory will be erased when the code protection is turned off.
4: When MCLR is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.
12.2 Calibration Bits

Brown-out Reset (BOR), Power-on Reset (POR) and 8 MHz internal oscillator (HFINTOSC) are factory calibrated. These calibration values are stored in fuses located in the Calibration Word (2009h). The Calibration Word is not erased when using the specified bulk erase sequence in the “PIC12F6XX/16F6XX Memory Programming Specification” (DS41244) and thus, does not require reprogramming.

12.3 Reset

The PIC12F683 differentiates between various kinds of Reset:

a) Power-on Reset (POR)
b) WDT Reset during normal operation
c) WDT Reset during Sleep
d) MCLR Reset during normal operation
e) MCLR Reset during Sleep
f) Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a “Reset state” on:

- Power-on Reset
- MCLR Reset
- MCLR Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

WDT wake-up does not cause register resets in the same manner as a WDT Reset since wake-up is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different Reset situations, as indicated in Table 12-2. Software can use these bits to determine the nature of the Reset. See Table 12-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 12-1.

The MCLR Reset path has a noise filter to detect and ignore small pulses. See Section 15.0 “Electrical Specifications” for pulse-width specifications.

FIGURE 12-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

Note 1: Refer to the Configuration Word register (Register 12-1).
12.3.1 POWER-ON RESET

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the POR, simply connect the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Section 15.0 “Electrical Specifications” for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until VDD reaches VBOD (see Section 12.3.4 “Brown-Out Reset (BOR)”).

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to the Application Note AN607, “Power-up Trouble Shooting” (DS00607).

12.3.2 MCLR

PIC12F683 has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

Voltages applied to the MCLR pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 12-2, is suggested.

An internal MCLR option is enabled by clearing the MCLRE bit in the Configuration Word register. When MCLRE = 0, the Reset signal to the chip is generated internally. When the MCLRE = 1, the GP3/MCLR pin becomes an external Reset input. In this mode, the GP3/MCLR pin has a weak pull-up to VDD.

12.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from the 31 kHz LFINTOSC oscillator. For more information, see Section 3.5 “Internal Clock Modes”. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A Configuration bit, PWRTEN, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip due to:

- VDD variation
- Temperature variation
- Process variation

See DC parameters for details (Section 15.0 “Electrical Specifications”).

Note: Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a “low” level to the MCLR pin, rather than pulling this pin directly to VSS.

---

**FIGURE 12-2: RECOMMENDED MCLR CIRCUIT**

![Recommended MCLR Circuit Diagram](image-url)
12.3.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register select one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = 01, the SBOREN bit of the PCON register enables/disables the BOR, allowing it to be controlled in software. By selecting BOREN<1:0> = 10, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 12-1 for the Configuration Word definition.

A brown-out occurs when VDD falls below VBOR for greater than parameter TBOR (see Section 15.0 “Electrical Specifications”). The brown-out condition will reset the device. This will occur regardless of VDD slew rate. A Brown-out Reset may not occur if VDD falls below VBOR for less than parameter TBOR.

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOR (see Figure 12-3). If enabled, the Power-up Timer will be invoked by the Reset and keep the chip in Reset an additional 64 ms.

If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

12.3.5 BOR CALIBRATION

The PIC12F683 stores the BOR calibration values in fuses located in the Calibration Word register (2008h). The Calibration Word register is not erased when using the specified bulk erase sequence in the “PIC12F6XX/16F6XX Memory Programming Specification” (DS41204) and thus, does not require reprogramming.

**Note:**
Address 2008h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See “PIC12F6XX/16F6XX Memory Programming Specification” (DS41204) for more information.

**FIGURE 12-3: BROWN-OUT SITUATIONS**

- **Note:** The Power-up Timer is enabled by the PWRTE bit in the Configuration Word register.

- **Note 1:** 64 ms delay only if PWRTE bit is programmed to ‘0’.
12.3.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

- PWRT time-out is invoked after POR has expired.
- OST is activated after the PWRT time-out has expired.

The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in EC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 12-4, Figure 12-5 and Figure 12-6 depict time-out sequences. The device can execute code from the INTOSC while OST is active by enabling Two-Speed Start-up or Fail-Safe Monitor (see Section 3.7.2 “Two-Speed Start-up Sequence” and Section 3.8 “Fail-Safe Clock Monitor”).

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then, bringing MCLR high will begin execution immediately (see Figure 12-5). This is useful for testing purposes or to synchronize more than one PIC12F683 device operating in parallel.

Table 12-5 shows the Reset conditions for some special registers, while Table 12-4 shows the Reset conditions for all the registers.

### TABLE 12-1: TIME-OUT IN VARIOUS SITUATIONS

<table>
<thead>
<tr>
<th>Oscillator Configuration</th>
<th>Power-up PWRT = 0</th>
<th>Brown-out Reset PWRT = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>XT, HS, LP</td>
<td>TPWRT + 1024 • TOSC</td>
<td>1024 • TOSC</td>
</tr>
<tr>
<td>RC, EC, INTOSC</td>
<td>TPWRT</td>
<td>—</td>
</tr>
</tbody>
</table>

### TABLE 12-2: STATUS/PCON Bits and Their Significance

<table>
<thead>
<tr>
<th>POR</th>
<th>BOR</th>
<th>TO</th>
<th>PD</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>1</td>
<td>1</td>
<td>Power-on Reset</td>
</tr>
<tr>
<td>u</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Brown-out Reset</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>0</td>
<td>u</td>
<td>WDT Reset</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>0</td>
<td>0</td>
<td>WDT Wake-up</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>u</td>
<td>u</td>
<td>MCLR Reset during normal operation</td>
</tr>
<tr>
<td>u</td>
<td>u</td>
<td>1</td>
<td>0</td>
<td>MCLR Reset during Sleep</td>
</tr>
</tbody>
</table>

Legend: u = unchanged, x = unknown

### TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT RESET

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 9</th>
<th>Bit 8</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG(2)</td>
<td>BOREN1</td>
<td>BOREN0</td>
<td>CP8</td>
<td>CP6</td>
<td>MCLRE</td>
<td>PWRTE</td>
<td>WDTE</td>
<td>FOSC2</td>
<td>FOSC1</td>
<td>FOSC0</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>PCON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>IP3</td>
<td>IP1</td>
<td>IP0</td>
<td>TO</td>
<td>PD</td>
<td>D</td>
<td>DC</td>
<td>C</td>
<td>0001 1xxx</td>
</tr>
</tbody>
</table>

Legend: u = unchanged, x = unknown, — = unimplemented bit, reads as ‘0’, q = value depends on condition. Shaded cells are not used by BOR.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

Note 2: See Configuration Word register (Register 12-1) for operation of all register bits.
### FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR)

- **VDD**
- **MCLR**
- **Internal POR**
- **PWRT Time-out**
- **OST Time-out**
- **Internal Reset**

- **TPWRT**
- **TOST**

### FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR)

- **VDD**
- **MCLR**
- **Internal POR**
- **PWRT Time-out**
- **OST Time-out**
- **Internal Reset**

- **TPWRT**
- **TOST**

### FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP (MCLR WITH VDD)

- **VDD**
- **MCLR**
- **Internal POR**
- **PWRT Time-out**
- **OST Time-out**
- **Internal Reset**

- **TPWRT**
- **TOST**
### TABLE 12-4: INITIALIZATION CONDITION FOR REGISTERS

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
<th>Power-on Reset</th>
<th>MCLR Reset</th>
<th>WDT Reset</th>
<th>Brown-out Reset&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>Wake-up from Sleep through Interrupt</th>
<th>Wake-up from Sleep through WDT Time-out</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>—</td>
<td>xxxxx xxxx</td>
<td></td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>INDF</td>
<td>00h/80h</td>
<td>xxxxx xxxx</td>
<td>xxxxx xxxx</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>TMR0</td>
<td>01h</td>
<td>xxxxx xxxx</td>
<td>uuuu</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>PCL</td>
<td>02h/82h</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td></td>
<td></td>
<td></td>
<td>PC + 1&lt;sup&gt;(3)&lt;/sup&gt;</td>
</tr>
<tr>
<td>STATUS</td>
<td>03h/83h</td>
<td>0001 lxxxx</td>
<td>000q quuu</td>
<td></td>
<td></td>
<td></td>
<td>quuq quuu&lt;sup&gt;(4)&lt;/sup&gt;</td>
</tr>
<tr>
<td>FSR</td>
<td>04h/84h</td>
<td>xxxxx xxxx</td>
<td>uuuu</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>GPIO</td>
<td>05h</td>
<td>--x0 x000</td>
<td>--x0 x000</td>
<td></td>
<td></td>
<td></td>
<td>-uu uu</td>
</tr>
<tr>
<td>PCLATH</td>
<td>0Ah/8Ah</td>
<td>--0 0 0000</td>
<td>--0 0 0000</td>
<td></td>
<td></td>
<td></td>
<td>-uu uu</td>
</tr>
<tr>
<td>INTCON</td>
<td>0Bh/8Bh</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td></td>
<td></td>
<td></td>
<td>uuuu uuuu&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td>PIR1</td>
<td>0Ch</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td></td>
<td></td>
<td></td>
<td>uuuu uuuu&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td>TMR1L</td>
<td>0Eh</td>
<td>xxxxx xxxx</td>
<td>uuuu</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>TMR1H</td>
<td>0Fh</td>
<td>xxxxx xxxx</td>
<td>uuuu</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>T1CON</td>
<td>10h</td>
<td>0000 0000</td>
<td>uuuu</td>
<td></td>
<td></td>
<td></td>
<td>-uu uu</td>
</tr>
<tr>
<td>TMR2</td>
<td>11h</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td></td>
<td></td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>T2CON</td>
<td>12h</td>
<td>-00 0000</td>
<td>-00 0000</td>
<td></td>
<td></td>
<td></td>
<td>-uu uu</td>
</tr>
<tr>
<td>CCP1L</td>
<td>13h</td>
<td>xxxxx xxxx</td>
<td>uuuu</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>CCP1H</td>
<td>14h</td>
<td>xxxxx xxxx</td>
<td>uuuu</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>CCP1CON</td>
<td>15h</td>
<td>--0 0 0000</td>
<td>--0 0 0000</td>
<td></td>
<td></td>
<td></td>
<td>-uu uu</td>
</tr>
<tr>
<td>WDTCON</td>
<td>18h</td>
<td>--0 1000</td>
<td>--0 1000</td>
<td></td>
<td></td>
<td></td>
<td>-uu uu</td>
</tr>
<tr>
<td>CMCON0</td>
<td>19h</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td></td>
<td></td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>CMCON1</td>
<td>20h</td>
<td>----- --10</td>
<td>----- --10</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>ADRESH</td>
<td>1Ah</td>
<td>xxxxx xxxx</td>
<td>uuuuu</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>ADCON0</td>
<td>1Bh</td>
<td>00-- 0000</td>
<td>00-- 0000</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>1Ch</td>
<td>1111 1111</td>
<td>1111 1111</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>TRISIO</td>
<td>1Dh</td>
<td>---1 1111</td>
<td>---1 1111</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>PIE1</td>
<td>1Eh</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>PCON</td>
<td>1Fh</td>
<td>00-- 0000</td>
<td>00-- 0000</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>OSCCON</td>
<td>20h</td>
<td>--0 1 --0x</td>
<td>--0u --uu</td>
<td></td>
<td>--uu --uu</td>
<td></td>
<td>--uu --uu</td>
</tr>
<tr>
<td>OSCTUNE</td>
<td>21h</td>
<td>--11 0q000</td>
<td>--11 0q000</td>
<td></td>
<td>--uu uu uu</td>
<td></td>
<td>--uu uu uu</td>
</tr>
<tr>
<td>PR2</td>
<td>22h</td>
<td>1111 1111</td>
<td>1111 1111</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>WPU</td>
<td>23h</td>
<td>--11 -1111</td>
<td>--11 -1111</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>IOC</td>
<td>24h</td>
<td>--0 0000</td>
<td>--0 0000</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>VRCON</td>
<td>25h</td>
<td>0--0 0000</td>
<td>0--0 0000</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>EEDAT</td>
<td>26h</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
<tr>
<td>EEDADR</td>
<td>27h</td>
<td>0000 0000</td>
<td>0000 0000</td>
<td></td>
<td>uuuu uuuu</td>
<td></td>
<td>uuuu uuuu</td>
</tr>
</tbody>
</table>

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as ‘0’, q = value depends on condition.

**Note 1:** If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

**Note 2:** One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

**Note 3:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**Note 4:** See Table 12-5 for Reset value for specific condition.

**Note 5:** If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.
### TABLE 12-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
<th>Power-on Reset</th>
<th>MCLR Reset</th>
<th>WDT Reset</th>
<th>Brown-out Reset</th>
<th>Wake-up from Sleep</th>
<th>Wake-up from Sleep through WDT Time-out</th>
</tr>
</thead>
<tbody>
<tr>
<td>EECON1</td>
<td>9Ch</td>
<td>---- x000</td>
<td>---- q000</td>
<td>---- q000</td>
<td>---- uuuu</td>
<td>---- uuuu</td>
<td></td>
</tr>
<tr>
<td>EECON2</td>
<td>9Dh</td>
<td>---- ---- ----</td>
<td>---- ----</td>
<td>---- ----</td>
<td>---- ----</td>
<td>---- ----</td>
<td></td>
</tr>
<tr>
<td>ADRESL</td>
<td>9Eh</td>
<td>xxxx xxxx</td>
<td>uuuu uuuu</td>
<td>uuuu uuuu</td>
<td>uuuu uuuu</td>
<td>uuuu uuuu</td>
<td></td>
</tr>
<tr>
<td>ANSEL</td>
<td>9Fh</td>
<td>-000 1111</td>
<td>-000 1111</td>
<td>-000 1111</td>
<td>-000 1111</td>
<td>-000 1111</td>
<td></td>
</tr>
</tbody>
</table>

Legend:  
- \(u\) = unchanged,  
- \(x\) = unknown,  
- – = unimplemented bit, reads as '0',  
- \(q\) = value depends on condition.

Note 1: If \(VDD\) goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 12-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

### TABLE 12-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

<table>
<thead>
<tr>
<th>Condition</th>
<th>Program Counter</th>
<th>Status Register</th>
<th>PCON Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-on Reset</td>
<td>000h</td>
<td>0001 1xxx</td>
<td>--01 --0x</td>
</tr>
<tr>
<td>MCLR Reset during Normal Operation</td>
<td>000h</td>
<td>000u uuuu</td>
<td>--0u --uu</td>
</tr>
<tr>
<td>MCLR Reset during Sleep</td>
<td>000h</td>
<td>0001 0uuu</td>
<td>--0u --uu</td>
</tr>
<tr>
<td>WDT Reset</td>
<td>000h</td>
<td>0000 uuuu</td>
<td>--0u --uu</td>
</tr>
<tr>
<td>WDT Wake-up</td>
<td>PC + 1</td>
<td>uuu0 0uuu</td>
<td>--uu --uu</td>
</tr>
<tr>
<td>Brown-out Reset</td>
<td>000h</td>
<td>0001 1uuu</td>
<td>--01 --10</td>
</tr>
<tr>
<td>Interrupt Wake-up from Sleep</td>
<td>PC + 1(1)</td>
<td>uuu1 0uuu</td>
<td>--uu --uu</td>
</tr>
</tbody>
</table>

Legend:  
- \(u\) = unchanged,  
- \(x\) = unknown,  
- – = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.
12.4 Interrupts

The PIC12F683 has multiple interrupt sources:

- External Interrupt GP2/INT
- Timer0 Overflow Interrupt
- GPIO Change Interrupts
- Comparator Interrupt
- A/D Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Register 1 (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

The Global Interrupt Enable bit, GIE of the INTCON register, enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIE1 register. GIE is cleared on Reset.

When an interrupt is serviced, the following actions occur automatically:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

The Return from Interrupt instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- GPIO Change Interrupt
- Timer0 Overflow Interrupt

The peripheral interrupt flags are contained in the PIR1 register. The corresponding interrupt enable bit is contained in the PIE1 register.

The following interrupt flags are contained in the PIR1 register:

- EEPROM Data Write Interrupt
- A/D Interrupt
- Comparator Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

For external interrupt events, such as the INT pin or GPIO change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 12-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1: Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, ADC, data EEPROM or Enhanced CCP modules, refer to the respective peripheral section.

12.4.1 GP2/INT INTERRUPT

The external interrupt on the GP2/INT pin is edge-triggered; either on the rising edge if the INTEDG bit of the OPTION register is set, or the falling edge, if the INTEDG bit is clear. When a valid edge appears on the GP2/INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared by software in the Interrupt Service Routine before re-enabling this interrupt. The GP2/INT interrupt can wake-up the processor from Sleep, if the INTE bit was set prior to going into Sleep. See Section 12.7 “Power-Down Mode (Sleep)” for details on Sleep and Figure 12-10 for timing of wake-up from Sleep through GP2/INT interrupt.

Note: The ANSEL and CMCON0 registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’ and cannot generate an interrupt.
12.4.2 TIMER0 INTERRUPT
An overflow (FFh → 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing the T0IE bit of the INTCON register. See Section 5.0 “Timer0 Module” for operation of the Timer0 module.

12.4.3 GPIO INTERRUPT
An input change on GPIO change sets the GPIF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing the GPIE bit of the INTCON register. Plus, individual pins can be configured through the IOC register.

**Note:** If a change on the I/O pin should occur when any GPIO operation is being executed, then the GPIF interrupt flag may not get set.

**FIGURE 12-7: INTERRUPT LOGIC**
FIGURE 12-8: INT PIN INTERRUPT TIMING

TABLE 12-6: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTCON</td>
<td>GIE</td>
<td>PEIE</td>
<td>T0IE</td>
<td>INTE</td>
<td>GPIE</td>
<td>T0IF</td>
<td>INTF</td>
<td>GPIF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>IOC</td>
<td>—</td>
<td>—</td>
<td>IOC5</td>
<td>IOC4</td>
<td>IOC3</td>
<td>IOC2</td>
<td>IOC1</td>
<td>IOC0</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>PIR1</td>
<td>EEIF</td>
<td>ADIF</td>
<td>CCP1IF</td>
<td>—</td>
<td>CMIF</td>
<td>OSFIF</td>
<td>TMR2IF</td>
<td>TMR1IF</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
<tr>
<td>PIE1</td>
<td>EEIE</td>
<td>ADIE</td>
<td>CCP1IE</td>
<td>—</td>
<td>CMIE</td>
<td>OSFIE</td>
<td>TMR2IE</td>
<td>TMR1IE</td>
<td>0000 0000</td>
<td>0000 0000</td>
</tr>
</tbody>
</table>

Legend: *x* = unknown, *u* = unchanged, *—* = unimplemented read as "0", *q* = value depends upon condition.

Shaded cells are not used by the interrupt module.

Note 1: INTF flag is sampled here (every Q1).
2: Asynchronous interrupt latency = 3-4 TCY. Synchronous latency = 3 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.
3: CLKOUT is available only in INTOSC and RC Oscillator modes.
4: For minimum width of INT pulse, refer to AC specifications in **Section 15.0 “Electrical Specifications”**.
5: INTF is enabled to be set any time during the Q4-Q1 cycles.
12.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Since the lower 16 bytes of all banks are common in the PIC12F683 (see Figure 2-2), temporary holding registers, W_TEMP and STATUS_TEMP, should be placed in here. These 16 locations do not require banking and therefore, makes it easier to context save and restore. The same code shown in Example 12-1 can be used to:

- Store the W register.
- Store the STATUS register.
- Execute the ISR code.
- Restore the Status (and Bank Select Bit register).
- Restore the W register.

**EXAMPLE 12-1: SAVING STATUS AND W REGISTERS IN RAM**

```
MOVWF W_TEMP ;Copy W to TEMP register
SWAPF STATUS, W ;Swap status to be saved into W
;Swaps are used because they do not affect the status bits
MOVWF STATUS_TEMP ;Save status to bank zero STATUS_TEMP register :
:(ISR) ;Insert user code here :
SWAPF STATUS_TEMP, W ;Swap STATUS_TEMP register into W ;(sets bank to original state)
MOVWF STATUS ;Move W into STATUS register
SWAPF W_TEMP, F ;Swap W_TEMP
SWAPF W_TEMP, W ;Swap W_TEMP into W
```

*Note:* The PIC12F683 normally does not require saving the PCLATH. However, if computed GOTO's are used in the ISR and the main code, the PCLATH must be saved and restored in the ISR.


12.6 Watchdog Timer (WDT)

The WDT has the following features:
- Operates from the LFINTOSC (31 kHz)
- Contains a 16-bit prescaler
- Shares an 8-bit prescaler with Timer0
- Time-out period is from 1 ms to 268 seconds
- Configuration bit and software controlled

WDT is cleared under certain conditions described in Table 12-7.

12.6.1 WDT OSCILLATOR

The WDT derives its time base from the 31 kHz LFINTOSC. The LTS bit of the OSCCON register does not reflect that the LFINTOSC is enabled.

The value of WDTCON is ‘---0 1000’ on all Resets. This gives a nominal time base of 17 ms.

**Note:** When the Oscillator Start-up Timer (OST) is invoked, the WDT is held in Reset, because the WDT Ripple Counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDT will begin counting (if enabled).

12.6.2 WDT CONTROL

The WDTE bit is located in the Configuration Word register. When set, the WDT runs continuously.

When the WDTE bit in the Configuration Word register is set, the SWDTEN bit of the WDTCON register has no effect. If WDTE is clear, then the SWDTEN bit can be used to enable and disable the WDT. Setting the bit will enable it and clearing the bit will disable it.

The PSA and PS<2:0> bits of the OPTION register have the same function as in previous versions of the PIC12F683 Family of microcontrollers. See Section 5.0 “Timer0 Module” for more information.

---

**FIGURE 12-9: WATCHDOG TIMER BLOCK DIAGRAM**

---

**TABLE 12-7: WDT STATUS**

<table>
<thead>
<tr>
<th>Conditions</th>
<th>WDT</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDTE = 0</td>
<td>Cleared</td>
</tr>
<tr>
<td>CLRWD Command</td>
<td></td>
</tr>
<tr>
<td>Oscillator Fail Detected</td>
<td></td>
</tr>
<tr>
<td>Exit Sleep + System Clock = T1OSC, EXTRC, INTRC, EXTCLK</td>
<td>Cleared until the end of OST</td>
</tr>
<tr>
<td>Exit Sleep + System Clock = XT, HS, LP</td>
<td></td>
</tr>
</tbody>
</table>
TABLE 12-8: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

REGISTER 12-2: WDTCN: WATCHDOG TIMER CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit 7-5</th>
<th>Bit 4-1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unimplemented: Read as ‘0’</td>
<td>WDTPS&lt;3:0&gt;: Watchdog Timer Period Select bits</td>
<td>SWDTEN: Software Enable or Disable the Watchdog Timer(1)</td>
</tr>
<tr>
<td>0000 = 1:32</td>
<td>0001 = 1:64</td>
<td>1 = WDT is turned on</td>
</tr>
<tr>
<td>0010 = 1:128</td>
<td>0011 = 1:256</td>
<td>0 = WDT is turned off (Reset value)</td>
</tr>
<tr>
<td>0100 = 1:512 (Reset value)</td>
<td>0101 = 1:1024</td>
<td></td>
</tr>
<tr>
<td>0110 = 1:2048</td>
<td>0111 = 1:4096</td>
<td></td>
</tr>
<tr>
<td>1000 = 1:8192</td>
<td>1001 = 1:16384</td>
<td></td>
</tr>
<tr>
<td>1010 = 1:32768</td>
<td>1011 = 1:65536</td>
<td></td>
</tr>
<tr>
<td>1100 = Reserved</td>
<td>1101 = Reserved</td>
<td></td>
</tr>
<tr>
<td>1110 = Reserved</td>
<td>1111 = Reserved</td>
<td></td>
</tr>
</tbody>
</table>

bit 0
**SWDTEN**: Software Enable or Disable the Watchdog Timer(1)

1 = WDT is turned on
0 = WDT is turned off (Reset value)

Note 1: If WDTE Configuration bit = 1, then WDT is always enabled, irrespective of this control bit. If WDTE Configuration bit = 0, then it is possible to turn WDT on/off with this control bit.

TABLE 12-8: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR, BOR</th>
<th>Value on all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDTCN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>WDTPS3</td>
<td>WDTPS2</td>
<td>WSTPS1</td>
<td>WDTPS0</td>
<td>SWDTEN</td>
<td>—</td>
</tr>
<tr>
<td>OPTION_REG</td>
<td>GPPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
<tr>
<td>CONFIG</td>
<td>CPD</td>
<td>CP</td>
<td>MCLRE</td>
<td>PWRT</td>
<td>WDTE</td>
<td>FOSC2</td>
<td>FOSC1</td>
<td>FOSC0</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Register 12-1 for operation of all Configuration Word register bits.
12.7 Power-Down Mode (Sleep)

The Power-down mode is entered by executing a SLEEP instruction.

If the Watchdog Timer is enabled:
- WDT will be cleared but keeps running.
- PD bit in the STATUS register is cleared.
- TO bit is set.
- Oscillator driver is turned off.
- I/O ports maintain the status they had before SLEEP was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSS, with no external circuitry drawing current from the I/O pin and the comparators and CVREF should be disabled. I/O pins that are high-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on GPIO should be considered.

The MCLR pin must be at a logic high level.

12.7.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:
1. External Reset input on MCLR pin.
2. Watchdog Timer wake-up (if WDT was enabled).
3. Interrupt from GP2/INT pin, GPIO change or a peripheral interrupt.

The first event will cause a device Reset. The two latter events are considered a continuation of program execution. The TO and PD bits in the STATUS register can be used to determine the cause of a device Reset. The PD bit, which is set on power-up, is cleared when Sleep is invoked. TO bit is cleared if WDT wake-up occurred.

The following peripheral interrupts can wake the device from Sleep:
1. Timer1 interrupt. Timer1 must be operating as an asynchronous counter.
2. ECCP Capture mode interrupt.
3. A/D conversion (when A/D clock source is FRC).
4. EEPROM write operation completion.
5. Comparator output changes state.
6. Interrupt-on-change.
7. External Interrupt from INT pin.

Other peripherals cannot generate interrupts since during Sleep, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

12.7.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bits set, one of the following will occur:
- If the interrupt occurs before the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will not be cleared, the TO bit will not be set and the PD bit will not be cleared.
- If the interrupt occurs during or after the execution of a SLEEP instruction, the device will immediately wake-up from Sleep. The SLEEP instruction is executed. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will be cleared, the TO bit will be set and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction. See Figure 12-10 for more details.
12.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note: The entire data EEPROM and Flash program memory will be erased when the code protection is turned off. See the "PIC12F6XX/16F6XX Memory Programming Specification" (DS41204) for more information.

12.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.
12.10 In-Circuit Serial Programming™

The PIC12F683 microcontrollers can be serially programmed while in the end application circuit. This is simply done with five connections for:

- clock
- data
- power
- ground
- programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the GP0 and GP1 pins low, while raising the MCLR (VPP) pin from VIL to VIHH. See the “PIC12F6XX/16F6XX Memory Programming Specification” (DS41204) for more information. GP0 becomes the programming data and GP1 becomes the programming clock. Both GP0 and GP1 are Schmitt Trigger inputs in Program/Verify mode.

A typical In-Circuit Serial Programming connection is shown in Figure 12-11.

**FIGURE 12-11: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION**

12.11 In-Circuit Debugger

Since in-circuit debugging requires access to three pins, MPLAB® ICD 2 development with a 14-pin device is not practical. A special 14-pin PIC12F683 ICD device is used with MPLAB ICD 2 to provide separate clock, data and MCLR pins and frees all normally available pins to the user.

A special debugging adapter allows the ICD device to be used in place of a PIC12F683 device. The debugging adapter is the only source of the ICD device.

When the ICD pin on the PIC12F683 ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 12-9 shows which features are consumed by the background debugger.

**TABLE 12-9: DEBUGGER RESOURCES**

<table>
<thead>
<tr>
<th>Resource</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stack</td>
<td>1 level</td>
</tr>
<tr>
<td>Program Memory</td>
<td>Address 0h must be NOP</td>
</tr>
<tr>
<td></td>
<td>700h-7FFh</td>
</tr>
</tbody>
</table>

For more information, see “MPLAB® ICD 2 In-Circuit Debugger User’s Guide” (DS51331), available on Microchip's web site (www.microchip.com).

**FIGURE 12-12: 14-PIN ICD PINOUT**

14-Pin PDIP

In-Circuit Debug Device

- NC
- ICDMCLR
- Vdd
- Vss
- MCLR/VPP/GP3
- GP1
- GP0
- ICDDATA
- GND
- GP5
- GP4
- GP3
- GP2
- GP1
- NC

* Isolation devices (as required)
13.0 INSTRUCTION SET SUMMARY

The PIC12F683 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 13-1, while the various opcode fields are summarized in Table 13-1.

Table 13-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution time of 1 \( \mu \)s. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a **NOP**.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

13.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a CLRF PORTA instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended consequence of clearing the condition that set the RAIF flag.

**TABLE 13-1: OPCODE FIELD DESCRIPTIONS**

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>f</td>
<td>Register file address (0x00 to 0x7F)</td>
</tr>
<tr>
<td>W</td>
<td>Working register (accumulator)</td>
</tr>
<tr>
<td>b</td>
<td>Bit address within an 8-bit file register</td>
</tr>
<tr>
<td>k</td>
<td>Literal field, constant data or label</td>
</tr>
<tr>
<td>x</td>
<td>Don’t care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.</td>
</tr>
<tr>
<td>d</td>
<td>Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.</td>
</tr>
<tr>
<td>PC</td>
<td>Program Counter</td>
</tr>
<tr>
<td>TO</td>
<td>Time-out bit</td>
</tr>
<tr>
<td>C</td>
<td>Carry bit</td>
</tr>
<tr>
<td>DC</td>
<td>Digit carry bit</td>
</tr>
<tr>
<td>Z</td>
<td>Zero bit</td>
</tr>
<tr>
<td>PD</td>
<td>Power-down bit</td>
</tr>
</tbody>
</table>

**FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS**

**Byte-oriented file register operations**

```
13 8 7 6 0
```

<table>
<thead>
<tr>
<th>OPCODE</th>
<th>d</th>
<th>f (FILE #)</th>
</tr>
</thead>
<tbody>
<tr>
<td>d = 0</td>
<td></td>
<td>for destination W</td>
</tr>
<tr>
<td>d = 1</td>
<td></td>
<td>for destination f</td>
</tr>
<tr>
<td>f = 7-bit file register address</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bit-oriented file register operations**

```
13 10 9 7 6 0
```

<table>
<thead>
<tr>
<th>OPCODE</th>
<th>b (BIT #)</th>
<th>f (FILE #)</th>
</tr>
</thead>
<tbody>
<tr>
<td>b = 3-bit bit address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f = 7-bit file register address</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Literal and control operations**

**General**

```
13 8 7 0
```

<table>
<thead>
<tr>
<th>OPCODE</th>
<th>k (literal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>k = 8-bit immediate value</td>
<td></td>
</tr>
</tbody>
</table>

**CALL and GOTO instructions only**

```
13 11 10 0
```

<table>
<thead>
<tr>
<th>OPCODE</th>
<th>k (literal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>k = 11-bit immediate value</td>
<td></td>
</tr>
</tbody>
</table>
TABLE 13-2: PIC12F683 INSTRUCTION SET

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>14-Bit Opcode</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>ADDWF, f, d</td>
<td>Add W and f</td>
<td>1</td>
<td>00</td>
<td>0111</td>
<td>dfff</td>
</tr>
<tr>
<td>ANDWF, f, d</td>
<td>AND W with f</td>
<td>1</td>
<td>00</td>
<td>0101</td>
<td>dfff</td>
</tr>
<tr>
<td>CLRf</td>
<td>Clear f</td>
<td>1</td>
<td>00</td>
<td>0001</td>
<td>lfff</td>
</tr>
<tr>
<td>CLRW</td>
<td>Clear W</td>
<td>1</td>
<td>00</td>
<td>0001</td>
<td>0xxx</td>
</tr>
<tr>
<td>COMF, f, d</td>
<td>Complement f</td>
<td>1</td>
<td>00</td>
<td>1001</td>
<td>dfff</td>
</tr>
<tr>
<td>DECf, f, d</td>
<td>Decrement f</td>
<td>1</td>
<td>00</td>
<td>0011</td>
<td>dfff</td>
</tr>
<tr>
<td>DECFSZ</td>
<td>Decrement f, Skip if 0</td>
<td>1(2)</td>
<td>00</td>
<td>1011</td>
<td>dfff</td>
</tr>
<tr>
<td>INCf, f, d</td>
<td>Increment f</td>
<td>1</td>
<td>00</td>
<td>1010</td>
<td>dfff</td>
</tr>
<tr>
<td>INCFSZ</td>
<td>Increment f, Skip if 0</td>
<td>1(2)</td>
<td>00</td>
<td>1111</td>
<td>dfff</td>
</tr>
<tr>
<td>IORWF, f, d</td>
<td>Inclusive OR W with f</td>
<td>1</td>
<td>00</td>
<td>0100</td>
<td>dfff</td>
</tr>
<tr>
<td>MOVf, f, d</td>
<td>Move f</td>
<td>1</td>
<td>00</td>
<td>1000</td>
<td>dfff</td>
</tr>
<tr>
<td>MOVWF, f</td>
<td>Move W to f</td>
<td>1</td>
<td>00</td>
<td>0000</td>
<td>lfff</td>
</tr>
<tr>
<td>NOP</td>
<td>No Operation</td>
<td>1</td>
<td>00</td>
<td>0000</td>
<td>0xxx</td>
</tr>
<tr>
<td>RLF, f, d</td>
<td>Rotate Left f through Carry</td>
<td>1</td>
<td>00</td>
<td>1101</td>
<td>dfff</td>
</tr>
<tr>
<td>RRF, f, d</td>
<td>Rotate Right f through Carry</td>
<td>1</td>
<td>00</td>
<td>1100</td>
<td>dfff</td>
</tr>
<tr>
<td>SUBWF, f, d</td>
<td>Subtract W from f</td>
<td>1</td>
<td>00</td>
<td>0010</td>
<td>dfff</td>
</tr>
<tr>
<td>SWAPF, f, d</td>
<td>Swap nibbles in f</td>
<td>1</td>
<td>00</td>
<td>1110</td>
<td>dfff</td>
</tr>
<tr>
<td>XORWF, f, d</td>
<td>Exclusive OR W with f</td>
<td>1</td>
<td>00</td>
<td>0110</td>
<td>dfff</td>
</tr>
</tbody>
</table>

BIT-ORIENTED FILE REGISTER OPERATIONS

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>14-Bit Opcode</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>BCF, f, b</td>
<td>Bit Clear f</td>
<td>1</td>
<td>01</td>
<td>00bb</td>
<td>bfff</td>
</tr>
<tr>
<td>BSF, f, b</td>
<td>Bit Set f</td>
<td>1</td>
<td>01</td>
<td>01bb</td>
<td>bfff</td>
</tr>
<tr>
<td>BTFSC, f, b</td>
<td>Bit Test f, Skip if Clear</td>
<td>1 (2)</td>
<td>01</td>
<td>10bb</td>
<td>bfff</td>
</tr>
<tr>
<td>BTFSs, f, b</td>
<td>Bit Test f, Skip if Set</td>
<td>1 (2)</td>
<td>01</td>
<td>11bb</td>
<td>bfff</td>
</tr>
</tbody>
</table>

LITERAL AND CONTROL OPERATIONS

<table>
<thead>
<tr>
<th>Mnemonic, Operands</th>
<th>Description</th>
<th>Cycles</th>
<th>14-Bit Opcode</th>
<th>Status Affected</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSb</td>
<td>LSb</td>
<td></td>
</tr>
<tr>
<td>ADDLW, k</td>
<td>Add literal and W</td>
<td>1</td>
<td>11</td>
<td>111x</td>
<td>kkkk</td>
</tr>
<tr>
<td>ANDLW, k</td>
<td>AND literal with W</td>
<td>1</td>
<td>11</td>
<td>1001</td>
<td>kkkk</td>
</tr>
<tr>
<td>CALL, k</td>
<td>Call Subroutine</td>
<td>2</td>
<td>10</td>
<td>0kkk</td>
<td>kkkk</td>
</tr>
<tr>
<td>CLRWDT</td>
<td>Clear Watchdog Timer</td>
<td>1</td>
<td>00</td>
<td>0000</td>
<td>0110</td>
</tr>
<tr>
<td>GOTO, k</td>
<td>Go to address</td>
<td>2</td>
<td>10</td>
<td>1kkk</td>
<td>kkkk</td>
</tr>
<tr>
<td>IORLW, k</td>
<td>Inclusive OR literal with W</td>
<td>1</td>
<td>11</td>
<td>1000</td>
<td>kkkk</td>
</tr>
<tr>
<td>MOVLW, k</td>
<td>Move literal to W</td>
<td>1</td>
<td>11</td>
<td>0xxx</td>
<td>kkkk</td>
</tr>
<tr>
<td>RETFIE</td>
<td>Return from interrupt</td>
<td>2</td>
<td>00</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>RETLW, k</td>
<td>Return with literal in W</td>
<td>2</td>
<td>11</td>
<td>01xx</td>
<td>kkkk</td>
</tr>
<tr>
<td>RETURN</td>
<td>Return from Subroutine</td>
<td>2</td>
<td>00</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>SLEEP</td>
<td>Go into Standby mode</td>
<td>1</td>
<td>00</td>
<td>0000</td>
<td>0110</td>
</tr>
<tr>
<td>SUBLW, k</td>
<td>Subtract W from literal</td>
<td>1</td>
<td>11</td>
<td>110x</td>
<td>kkkk</td>
</tr>
<tr>
<td>XORLW, k</td>
<td>Exclusive OR literal with W</td>
<td>1</td>
<td>11</td>
<td>1010</td>
<td>kkkk</td>
</tr>
</tbody>
</table>

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF GPIO, 1), the value used will be that value present on the pins themselves. For example, if the data latch is ‘1’ for a pin configured as input and is driven low by an external device, the data will be written back with a ‘0’.

2: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.
13.2 Instruction Descriptions

ADDLW  Add literal and W
Syntax: [ label ] ADDLW k
Operands: 0 ≤ k ≤ 255
Operation: (W) + k → (W)
Status Affected: C, DC, Z
Description: The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ADDWF  Add W and f
Syntax: [ label ] ADDWF f,d
Operands: 0 ≤ f ≤ 127
d ∈ [0,1]
Operation: (W) + (f) → (destination)
Status Affected: C, DC, Z
Description: Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW  AND literal with W
Syntax: [ label ] ANDLW k
Operands: 0 ≤ k ≤ 255
Operation: (W) .AND. (k) → (W)
Status Affected: Z
Description: The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

ANDWF  AND W with f
Syntax: [ label ] ANDWF f,d
Operands: 0 ≤ f ≤ 127
d ∈ [0,1]
Operation: (W) .AND. (f) → (destination)
Status Affected: Z
Description: AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF  Bit Clear f
Syntax: [ label ] BCF f,b
Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7
Operation: 0 → (f<b>)
Status Affected: None
Description: Bit ‘b’ in register ‘f’ is cleared.

BSF  Bit Set f
Syntax: [ label ] BSF f,b
Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7
Operation: 1 → (f<b>)
Status Affected: None
Description: Bit ‘b’ in register ‘f’ is set.

BTFSC  Bit Test f, Skip if Clear
Syntax: [ label ] BTFSC f,b
Operands: 0 ≤ f ≤ 127
0 ≤ b ≤ 7
Operation: skip if (f<b>) = 0
Status Affected: None
Description: If bit ‘b’ in register ‘f’ is ‘1’, the next instruction is executed. If bit ‘b’, in register ‘f’, is ‘0’, the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.
### BTFSS (Bit Test f, Skip if Set)

**Syntax:**
\[
\text{[ label]} \ \text{BTFSS} \ f,b
\]

**Operands:**
\[
0 \leq f \leq 127 \\
0 \leq b < 7
\]

**Operation:**
Skip if \((f<b>) = 1\)

**Status Affected:** None

**Description:**
If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

### CALL (Call Subroutine)

**Syntax:**
\[
\text{[ label]} \ \text{CALL} \ k
\]

**Operands:**
\[
0 \leq k \leq 2047
\]

**Operation:**
\[
(P_C)+1 \rightarrow \text{TOS}, \\
k \rightarrow \text{PC}<10:0>, \\
(P\text{CLAT}<4:3>) \rightarrow \text{PC}<12:11>
\]

**Status Affected:** None

**Description:**
Call Subroutine. First, return address \((P_C + 1)\) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

### CLRF (Clear f)

**Syntax:**
\[
\text{[ label]} \ \text{CLRF} \ f
\]

**Operands:**
\[
0 \leq f \leq 127
\]

**Operation:**
\[
00h \rightarrow (f) \\
1 \rightarrow Z
\]

**Status Affected:** Z

**Description:**
The contents of register 'f' are cleared and the Z bit is set.

### CLRW (Clear W)

**Syntax:**
\[
\text{[ label]} \ \text{CLRW}
\]

**Operands:** None

**Operation:**
\[
00h \rightarrow (W) \\
1 \rightarrow Z
\]

**Status Affected:** Z

**Description:**
W register is cleared. Zero bit (Z) is set.

### CLRWDT (Clear Watchdog Timer)

**Syntax:**
\[
\text{[ label]} \ \text{CLRWDT}
\]

**Operands:** None

**Operation:**
\[
00h \rightarrow \text{WDT} \\
0 \rightarrow \text{WDT prescaler}, \\
1 \rightarrow \text{TO} \\
1 \rightarrow \text{PD}
\]

**Status Affected:** TO, PD

**Description:**
CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits TO and PD are set.

### COMF (Complement f)

**Syntax:**
\[
\text{[ label]} \ \text{COMF} \ f,d
\]

**Operands:**
\[
0 \leq f \leq 127 \\
d \in [0,1]
\]

**Operation:**
\[
(f) \rightarrow (\text{destination})
\]

**Status Affected:** Z

**Description:**
The contents of register 'f' are complemented. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

### DECF (Decrement f)

**Syntax:**
\[
\text{[ label]} \ \text{DECF} \ f,d
\]

**Operands:**
\[
0 \leq f \leq 127 \\
d \in [0,1]
\]

**Operation:**
\[
(f) - 1 \rightarrow (\text{destination})
\]

**Status Affected:** Z

**Description:**
Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.
### DECFSZ

**Decrement f, Skip if 0**

**Syntax:**

\[
\text{[label]} \ DECFSZ \ f,d
\]

**Operands:**

\[
0 \leq f \leq 127 \\
\quad d \in [0,1]
\]

**Operation:**

\[
\text{(f)} - 1 \rightarrow \text{(destination)}; \\
\text{skip if result} = 0
\]

**Status Affected:** None

**Description:**

The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '0', the next instruction is executed. If the result is '1', a NOP is executed instead, making it a 2-cycle instruction.

### INCFSZ

**Increment f, Skip if 0**

**Syntax:**

\[
\text{[label]} \ INCFSZ \ f,d
\]

**Operands:**

\[
0 \leq f \leq 127 \\
\quad d \in [0,1]
\]

**Operation:**

\[
\text{(f)} + 1 \rightarrow \text{(destination)}; \\
\text{skip if result} = 0
\]

**Status Affected:** None

**Description:**

The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

### GOTO

**Unconditional Branch**

**Syntax:**

\[
\text{[label]} \ GOTO \ k
\]

**Operands:**

\[
0 \leq k \leq 2047
\]

**Operation:**

\[
k \rightarrow \text{PC}<10:0> \\
PCLATH<4:3> \rightarrow \text{PC}<12:11>
\]

**Status Affected:** None

**Description:**

GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

### INCF

**Increment f**

**Syntax:**

\[
\text{[label]} \ INCF \ f,d
\]

**Operands:**

\[
0 \leq f \leq 127 \\
\quad d \in [0,1]
\]

**Operation:**

\[
\text{(f)} + 1 \rightarrow \text{(destination)}
\]

**Status Affected:** Z

**Description:**

The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

### IORLW

**Inclusive OR literal with W**

**Syntax:**

\[
\text{[label]} \ IORLW \ k
\]

**Operands:**

\[
0 \leq k \leq 255
\]

**Operation:**

\[
(W) \ .OR. k \rightarrow (W)
\]

**Status Affected:** Z

**Description:**

The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

### IORWF

**Inclusive OR W with f**

**Syntax:**

\[
\text{[label]} \ IORWF \ f,d
\]

**Operands:**

\[
0 \leq f \leq 127 \\
\quad d \in [0,1]
\]

**Operation:**

\[
(W) \ .OR. (f) \rightarrow \text{(destination)}
\]

**Status Affected:** Z

**Description:**

Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.
**MOVF**  
**Move f**

**Syntax:** \([ label \] \) MOVF \ f, d

**Operands:**  
0 ≤ f ≤ 127  
d ∈ [0, 1]

**Operation:**  
(f) → (dest)

**Status Affected:**  
Z

**Description:**  
The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

**Words:** 1

**Cycles:** 1

**Example:**  
MOVF FSR, 0

After Instruction

\[
\begin{align*}
W &= \text{value in FSR register} \\
Z &= 1
\end{align*}
\]

**MOVF**  
**Move W to f**

**Syntax:** \([ label \] \) MOVWF \ f

**Operands:**  
0 ≤ f ≤ 127

**Operation:**  
(W) → (f)

**Status Affected:**  
None

**Description:**  
Move data from W register to register 'f'.

**Words:** 1

**Cycles:** 1

**Example:**  
MOVWF OPTION

Before Instruction

\[
\begin{align*}
\text{OPTION} &= 0xFF \\
W &= 0x4F
\end{align*}
\]

After Instruction

\[
\begin{align*}
\text{OPTION} &= 0x4F \\
W &= 0x4F
\end{align*}
\]

**MOVLW**  
**Move literal to W**

**Syntax:** \([ label \] \) MOVLW \ k

**Operands:**  
0 ≤ k ≤ 255

**Operation:**  
k → (W)

**Status Affected:**  
None

**Description:**  
The eight-bit literal 'k' is loaded into W register. The “don’t cares” will assemble as ‘0’ s.

**Words:** 1

**Cycles:** 1

**Example:**  
MOVLW 0x5A

After Instruction

\[
W = 0x5A
\]

**NOP**  
**No Operation**

**Syntax:** \([ label \] \) NOP

**Operands:**  
None

**Operation:**  
No operation

**Status Affected:**  
None

**Description:**  
No operation.

**Words:** 1

**Cycles:** 1

**Example:**  
NOP
### RETFIE

**Return from Interrupt**

| Syntax: | [ label ] RETFIE |
| Operands: | None |
| Operation: | TOS → PC, 1 → GIE |
| Status Affected: | None |
| Description: | Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction. |
| Words: | 1 |
| Cycles: | 2 |
| Example: | After Interrupt  
  PC = TOS  
  GIE = 1 |

### RETLW

**Return with literal in W**

| Syntax: | [ label ] RETLW k |
| Operands: | 0 ≤ k ≤ 255 |
| Operation: | k → (W); TOS → PC |
| Status Affected: | None |
| Description: | The W register is loaded with the eight bit literal ‘k’. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction. |
| Words: | 1 |
| Cycles: | 2 |
| Example: | CALL TABLE; W contains table  
  ; offset value  
  TABLE  
  ; W now has table value  
  ADDWF PC ; W = offset  
  RETLW k1 ; Begin table  
  RETLW k2 ;  
  RETLW kn ; End of table |

Before Instruction  
W = 0x07  
After Instruction  
W = value of k8 |

### RETURN

**Return from Subroutine**

| Syntax: | [ label ] RETURN |
| Operands: | None |
| Operation: | TOS → PC |
| Status Affected: | None |
| Description: | Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction. |
### RLF  Rotate Left f through Carry

**Syntax:**  
\[\text{\texttt{label}}\] RLF \(f,d\)

**Operands:**  
\(0 \leq f \leq 127\)  
\(d \in [0,1]\)

**Operation:**  
See description below

**Status Affected:**  
\(C\)

**Description:**  
The contents of register \(f\) are rotated one bit to the left through the Carry flag. If \(d\) is \(0\), the result is placed in the \(W\) register. If \(d\) is \(1\), the result is stored back in register \(f\).

| Words: | 1 |
| Cycles: | 1 |

**Example:**  
\[\text{RLF REG1,0}\]

**Before Instruction:**

- \(\text{REG1} = 1110\ 0110\)
- \(C = 0\)

**After Instruction:**

- \(\text{REG1} = 1110\ 0110\)
- \(\text{W} = 1100\ 1100\)
- \(C = 1\)

### SLEEP  Enter Sleep mode

**Syntax:**  
\[\text{\texttt{label}}\] SLEEP

**Operands:**  
None

**Operation:**  
00h \(\rightarrow\) WDT,  
0 \(\rightarrow\) WDT prescaler,  
1 \(\rightarrow\) \(\text{TO}\),  
0 \(\rightarrow\) \(\text{PD}\)

**Status Affected:**  
\(\text{TO, PD}\)

**Description:**  
The power-down Status bit, \(\text{PD}\) is cleared. Time-out Status bit, \(\text{TO}\) is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

### RRF  Rotate Right f through Carry

**Syntax:**  
\[\text{\texttt{label}}\] RRF \(f,d\)

**Operands:**  
\(0 \leq f \leq 127\)  
\(d \in [0,1]\)

**Operation:**  
See description below

**Status Affected:**  
\(C\)

**Description:**  
The contents of register \(f\) are rotated one bit to the right through the Carry flag. If \(d\) is \(0\), the result is placed in the \(W\) register. If \(d\) is \(1\), the result is placed back in register \(f\).

### SUBLW  Subtract W from literal

**Syntax:**  
\[\text{\texttt{label}}\] SUBLW \(k\)

**Operands:**  
\(0 \leq k \leq 255\)

**Operation:**  
\(k - (W) \rightarrow (W)\)

**Status Affected:**  
\(C, \text{DC}, Z\)

**Description:**  
The \(W\) register is subtracted (2's complement method) from the eight-bit literal \(k\). The result is placed in the \(W\) register.

| \(C = 0\) | \(W > k\) |
| \(C = 1\) | \(W \leq k\) |
| \(\text{DC} = 0\) | \(W < 3:0 > k < 3:0\) |
| \(\text{DC} = 1\) | \(W < 3:0 > \leq k < 3:0\) |
**SUBWF**  
**Subtract W from f**

Syntax:  
\[ label \] SUBWF f,d

Operands:  
\[ 0 \leq f \leq 127 \]
\[ d \in [0,1] \]

Operation:  
\( (f) \cdot (W) \rightarrow (\text{destination}) \)

Status Affected:  
C, DC, Z

Description:  
Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

| \( C = 0 \) | W > f |
| \( C = 1 \) | W ≤ f |
| \( DC = 0 \) | W<3:0> > f<3:0> |
| \( DC = 1 \) | W<3:0> ≤ f<3:0> |

**SWAPF**  
**Swap Nibbles in f**

Syntax:  
\[ label \] SWAPF f,d

Operands:  
\[ 0 \leq f \leq 127 \]
\[ d \in [0,1] \]

Operation:  
\( (f<3:0>) \rightarrow (\text{destination}<7:4>) \), \( (f<7:4>) \rightarrow (\text{destination}<3:0>) \)

Status Affected:  
None

Description:  
The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

**XORLW**  
**Exclusive OR literal with W**

Syntax:  
\[ label \] XORLW k

Operands:  
\[ 0 \leq k \leq 255 \]

Operation:  
\( (W) \cdot \text{XOR} \cdot k \rightarrow (W) \)

Status Affected:  
Z

Description:  
The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

**XORWF**  
**Exclusive OR W with f**

Syntax:  
\[ label \] XORWF f,d

Operands:  
\[ 0 \leq f \leq 127 \]
\[ d \in [0,1] \]

Operation:  
\( (W) \cdot \text{XOR} \cdot (f) \rightarrow (\text{destination}) \)

Status Affected:  
Z

Description:  
Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

© 2007 Microchip Technology Inc.
14.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C18 and MPLAB C30 C Compilers
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PICSTART® Plus Development Programmer
  - MPLAB PM3 Device Programmer
  - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (assembly or C)
  - Mixed assembly and C
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.
14.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:
- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

14.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

14.4 MPLINK Object Linker/
MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:
- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

14.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:
- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

14.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.
14.7 MPLAB ICE 2000
High-Performance
In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

14.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip’s next generation high-speed emulator for Microchip Flash DSC® and MCU devices. It debugging and programs PIC® and dsPIC® Flash microcontrollers with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer’s PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high speed, noise tolerant, low-voltage differential signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

14.9 MPLAB ICD 2 In-Circuit Debugger

Microchip’s In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip’s In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

14.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.
14.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

14.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip’s baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH’s PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip’s powerful, mid-range Flash memory family of microcontrollers.

14.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory. The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KeeLOQ® security ICs, CAN, IrDA®, PowerSmart® battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest “Product Selector Guide” (DS00148) for the complete list of demonstration, development and evaluation kits.
15.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias ................................................................................................. -40° to +125°C
Storage temperature .................................................................................................................... -65°C to +150°C
Voltage on VDD with respect to VSS ............................................................................................ -0.3V to +6.5V
Voltage on MCLR with respect to VSS ........................................................................................ -0.3V to +13.5V
Voltage on all other pins with respect to VSS ................................................................. -0.3V to (VDD + 0.3V)
Total power dissipation(†) ........................................................................................................ 800 mW
Maximum current out of VSS pin .......................................................................................... 95 mA
Maximum current into VDD pin .......................................................................................... 95 mA
Input clamp current, IIK (VI < 0 or VI > VDD)................................................................. ±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)................................................................. ±20 mA
Maximum output current sunk by any I/O pin .............................................................. 25 mA
Maximum output current sourced by any I/O pin .......................................................... 25 mA
Maximum current sunk by GPIO ...................................................................................... 90 mA
Maximum current sourced GPIO .................................................................................... 90 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = VDD \times (IDD - \sum IOH) + \sum (VDD - VOH) \times IOH + \sum (VOL \times IOL)$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.
FIGURE 15-1: PIC12F683 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 15-2: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE

Note 2: The shaded regions indicate the frequency accuracy ranges for different VDD and temperature conditions.
15.1 DC Characteristics: PIC12F683-I (Industrial)
PIC12F683-E (Extended)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D001</td>
<td>VDD</td>
<td>Supply Voltage</td>
<td>2.0</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>Fosc &lt; = 8 MHz: HFINTOSC, EC</td>
</tr>
<tr>
<td>D001C</td>
<td></td>
<td></td>
<td>2.0</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>Fosc &lt; = 4 MHz</td>
</tr>
<tr>
<td>D001D</td>
<td></td>
<td></td>
<td>3.0</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>Fosc &lt; = 10 MHz</td>
</tr>
<tr>
<td>D001D</td>
<td></td>
<td></td>
<td>4.5</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>Fosc &lt; = 20 MHz</td>
</tr>
<tr>
<td>D002*</td>
<td>VDR</td>
<td>RAM Data Retention Voltage(1)</td>
<td>1.5</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>Device in Sleep mode</td>
</tr>
<tr>
<td>D003</td>
<td>VPOR</td>
<td>VDD Start Voltage to ensure internal Power-on Reset signal</td>
<td>—</td>
<td>VSS</td>
<td>—</td>
<td>V</td>
<td>See Section 12.3.1 “Power-on Reset” for details.</td>
</tr>
<tr>
<td>D004*</td>
<td>SVDD</td>
<td>VDD Rise Rate to ensure internal Power-onReset signal</td>
<td>0.05</td>
<td>—</td>
<td>—</td>
<td>V/ms</td>
<td>See Section 12.3.1 “Power-on Reset” for details.</td>
</tr>
</tbody>
</table>

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.
15.2 DC Characteristics: PIC12F683-I (Industrial)
PIC12F683-E (Extended)

<table>
<thead>
<tr>
<th>DC CHARACTERISTICS</th>
<th>Standard Operating Conditions (unless otherwise stated)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Operating temperature (-40°C \leq TA \leq +85°C) for industrial (\leq +125°C) for extended</td>
</tr>
<tr>
<td><strong>Param No.</strong></td>
<td><strong>Device Characteristics</strong></td>
</tr>
<tr>
<td><strong>D010</strong></td>
<td>Supply Current ((I_{DD}))(^{(1, 2)})</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>D011*</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>D012</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>D013*</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>D014</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>D015</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>D016*</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>D017</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>D018</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>D019</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The test conditions for all \(I_{DD}\) measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to \(V_{DD}\); \(MCLR = V_{DD}\); WDT disabled.

**Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

**Note 3:** For RC oscillator configurations, current through \(R_{EXT}\) is not included. The current through the resistor can be extended by the formula \(I_R = \frac{V_{DD}}{2R_{EXT}}\) (mA) with \(R_{EXT}\) in k\(\Omega\).
## 15.3 DC Characteristics: PIC12F683-I (Industrial)

**DC CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Device Characteristics</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D020</td>
<td>Power-down Base Current(IPD)(2)</td>
<td>—</td>
<td>0.05</td>
<td>1.2</td>
<td>μA</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.15</td>
<td>1.5</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.35</td>
<td>1.8</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>150</td>
<td>500</td>
<td>nA</td>
<td>3.0</td>
</tr>
<tr>
<td>D021</td>
<td>— 1.0 2.2 μA 2.0 WDT Current(1)</td>
<td>—</td>
<td>2.0</td>
<td>4.0</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>3.0</td>
<td>7.0</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D022</td>
<td>— 42 60 μA 3.0 BOR Current(1)</td>
<td>—</td>
<td>85</td>
<td>122</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D023</td>
<td>— 32 45 μA 2.0 Comparator Current(1), both comparators enabled</td>
<td>—</td>
<td>60</td>
<td>78</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>120</td>
<td>160</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D024</td>
<td>— 30 36 μA 2.0 CVREF Current(1) (high range)</td>
<td>—</td>
<td>45</td>
<td>55</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>75</td>
<td>95</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D025†</td>
<td>— 39 47 μA 2.0 CVREF Current(1) (low range)</td>
<td>—</td>
<td>59</td>
<td>72</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>98</td>
<td>124</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D026</td>
<td>— 4.5 7.0 μA 2.0 T1OSC Current(1), 32.768 kHz</td>
<td>—</td>
<td>5.0</td>
<td>8.0</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>6.0</td>
<td>12</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D027</td>
<td>— 0.30 1.6 μA 3.0 A/D Current(1), no conversion in progress</td>
<td>—</td>
<td>0.36</td>
<td>1.9</td>
<td>μA</td>
<td>5.0</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

**Note 2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.
## DC Characteristics: PIC12F683-E (Extended)

### DC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Device Characteristics</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D020E</td>
<td>Power-down Base Current (IPD)&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>—</td>
<td>0.05</td>
<td>9</td>
<td>μA</td>
<td>2.0 WDT, BOR, Comparators, VREF and T1OSC disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.15</td>
<td>11</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.35</td>
<td>15</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D021E</td>
<td></td>
<td>—</td>
<td>1</td>
<td>17.5</td>
<td>μA</td>
<td>2.0 WDT Current&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>2</td>
<td>19</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>3</td>
<td>22</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D022E</td>
<td></td>
<td>—</td>
<td>42</td>
<td>65</td>
<td>μA</td>
<td>3.0 BOR Current&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>85</td>
<td>127</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D023E</td>
<td></td>
<td>—</td>
<td>32</td>
<td>45</td>
<td>μA</td>
<td>2.0 Comparator Current&lt;sup&gt;(1)&lt;/sup&gt;, both comparators enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>60</td>
<td>78</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>120</td>
<td>160</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D024E</td>
<td></td>
<td>—</td>
<td>30</td>
<td>70</td>
<td>μA</td>
<td>2.0 CVREF Current&lt;sup&gt;(1)&lt;/sup&gt; (high range)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>45</td>
<td>90</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>75</td>
<td>120</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D025E*</td>
<td></td>
<td>—</td>
<td>39</td>
<td>91</td>
<td>μA</td>
<td>2.0 CVREF Current&lt;sup&gt;(1)&lt;/sup&gt; (low range)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>59</td>
<td>117</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>98</td>
<td>156</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D026E</td>
<td></td>
<td>—</td>
<td>4.5</td>
<td>25</td>
<td>μA</td>
<td>2.0 T1OSC Current&lt;sup&gt;(1)&lt;/sup&gt;, 32.768 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>5</td>
<td>30</td>
<td>μA</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>6</td>
<td>40</td>
<td>μA</td>
<td>5.0</td>
</tr>
<tr>
<td>D027E</td>
<td></td>
<td>—</td>
<td>0.30</td>
<td>12</td>
<td>μA</td>
<td>3.0 A/D Current&lt;sup&gt;(1)&lt;/sup&gt;, no conversion in progress</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.36</td>
<td>16</td>
<td>μA</td>
<td>5.0</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

**Note 2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.
## 15.5 DC Characteristics: PIC12F683-I (Industrial)  
PIC12F683-E (Extended)

### DC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D030</td>
<td>VIL</td>
<td>Input Low Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>I/O Port:</td>
<td></td>
<td>Vss</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>4.5 V ≤ Vdd ≤ 5.5 V</td>
</tr>
<tr>
<td>D030A</td>
<td>with TTL buffer</td>
<td></td>
<td>Vss</td>
<td>—</td>
<td>0.15 Vdd</td>
<td>V</td>
<td>2.0 V ≤ Vdd ≤ 4.5 V</td>
</tr>
<tr>
<td>D031</td>
<td>VIL</td>
<td>Input Low Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>I/O Port:</td>
<td></td>
<td>Vss</td>
<td>—</td>
<td>0.2 Vdd</td>
<td>V</td>
<td>2.0 V ≤ Vdd ≤ 5.5 V</td>
</tr>
<tr>
<td>D032</td>
<td>MCLR, OSC1 (RC mode)</td>
<td></td>
<td>Vss</td>
<td>—</td>
<td>0.2 Vdd</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D033</td>
<td>OSC1 (XT and LP modes)</td>
<td></td>
<td>Vss</td>
<td>—</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D033A</td>
<td>OSC1 (HS mode)</td>
<td></td>
<td>Vss</td>
<td>—</td>
<td>0.3 Vdd</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D040</td>
<td>VIH</td>
<td>Input High Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>I/O ports:</td>
<td></td>
<td>2.0</td>
<td>—</td>
<td>Vdd</td>
<td>V</td>
<td>4.5 V ≤ Vdd ≤ 5.5 V</td>
</tr>
<tr>
<td>D040A</td>
<td>with TTL buffer</td>
<td></td>
<td>0.25 Vdd + 0.8</td>
<td>—</td>
<td>Vdd</td>
<td>V</td>
<td>2.0 V ≤ Vdd ≤ 4.5 V</td>
</tr>
<tr>
<td>D041</td>
<td>VIH</td>
<td>Input High Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>I/O ports:</td>
<td></td>
<td>0.8 Vdd</td>
<td>—</td>
<td>Vdd</td>
<td>V</td>
<td>2.0 V ≤ Vdd ≤ 5.5 V</td>
</tr>
<tr>
<td>D042</td>
<td>MCLR</td>
<td></td>
<td>0.8 Vdd</td>
<td>—</td>
<td>Vdd</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D043</td>
<td>OSC1 (XT and LP modes)</td>
<td></td>
<td>1.6</td>
<td>—</td>
<td>Vdd</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D043A</td>
<td>OSC1 (HS mode)</td>
<td></td>
<td>0.7 Vdd</td>
<td>—</td>
<td>Vdd</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D043B</td>
<td>OSC1 (RC mode)</td>
<td></td>
<td>0.9 Vdd</td>
<td>—</td>
<td>Vdd</td>
<td>V</td>
<td>(Note 1)</td>
</tr>
<tr>
<td>D060</td>
<td>IIL</td>
<td>Input Leakage Current(2)</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>I/O ports:</td>
<td></td>
<td>± 0.1</td>
<td>± 1</td>
<td>VSS ≤ VPIN ≤ Vdd, Pin at high-impedance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D061</td>
<td>MCLR(3)</td>
<td></td>
<td>± 0.1</td>
<td>± 5</td>
<td>µA</td>
<td>VSS ≤ VPIN ≤ Vdd</td>
<td></td>
</tr>
<tr>
<td>D063</td>
<td>OSC1</td>
<td></td>
<td>± 0.1</td>
<td>± 5</td>
<td>µA</td>
<td>VSS ≤ VPIN ≤ Vdd, XT, HS and LP oscillator configuration</td>
<td></td>
</tr>
<tr>
<td>D070*</td>
<td>IPUR</td>
<td>GPIO Weak Pull-up Current</td>
<td>50</td>
<td></td>
<td>250</td>
<td>400</td>
<td>µA</td>
</tr>
<tr>
<td>D080</td>
<td>VOL</td>
<td>Output Low Voltage(5)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>I/O ports:</td>
<td></td>
<td>—</td>
<td>—</td>
<td>0.6</td>
<td>V</td>
<td>IOL = 8.5 mA, VDD = 4.5 V (Ind.)</td>
</tr>
<tr>
<td>D090</td>
<td>VOH</td>
<td>Output High Voltage(5)</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>I/O ports:</td>
<td></td>
<td>VDD – 0.7</td>
<td>—</td>
<td>—</td>
<td>µA</td>
<td>ICH = -3.0 mA, VDD = 4.5 V (Ind.)</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.  
† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.  

**Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.  
2: Negative current is defined as current sourced by the pin.  
3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.  
4: See Section 10.4.1 “Using the Data EEPROM” for additional information.  
5: Including OSC2 in CLKOUT mode.
### 15.5 DC Characteristics: PIC12F683-I (Industrial) PIC12F683-E (Extended) (Continued)

#### DC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D100</td>
<td>IULP</td>
<td>Ultra Low-Power Wake-Up Current</td>
<td>—</td>
<td>200</td>
<td>—</td>
<td>nA</td>
<td>See Application Note AN879, “Using the Microchip Ultra Low-Power Wake-up Module” (DS00879)</td>
</tr>
<tr>
<td>D101*</td>
<td>COSC2</td>
<td>Capacitive Loading Specs on Output Pins</td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>pF</td>
<td>In XT, HS and LP modes when external clock is used to drive OSC1</td>
</tr>
<tr>
<td>D101A*</td>
<td>C/O</td>
<td>All I/O pins</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>D120</td>
<td>Ed</td>
<td>Byte Endurance</td>
<td>100K</td>
<td>1M</td>
<td>—</td>
<td>E/W</td>
<td>-40°C ≤ TA ≤ +85°C</td>
</tr>
<tr>
<td>D120A</td>
<td>Ed</td>
<td>Byte Endurance</td>
<td>10K</td>
<td>100K</td>
<td>—</td>
<td>E/W</td>
<td>+85°C ≤ TA ≤ +125°C</td>
</tr>
<tr>
<td>D121</td>
<td>VDRW</td>
<td>VDD for Read/Write</td>
<td>VMIN</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>Using EECON1 to read/write VMIN = Minimum operating voltage</td>
</tr>
<tr>
<td>D122</td>
<td>TDEW</td>
<td>Erase/Write Cycle Time</td>
<td>—</td>
<td>5</td>
<td>6</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>D123</td>
<td>TRETD</td>
<td>Characteristic Retention</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>Year</td>
<td>Provided no other specifications are violated</td>
</tr>
<tr>
<td>D124</td>
<td>TREF</td>
<td>Number of Total Erase/Write Cycles before Refresh(4)</td>
<td>1M</td>
<td>10M</td>
<td>—</td>
<td>E/W</td>
<td>-40°C ≤ TA ≤ +85°C</td>
</tr>
<tr>
<td>D130</td>
<td>EP</td>
<td>Cell Endurance</td>
<td>10K</td>
<td>100K</td>
<td>—</td>
<td>E/W</td>
<td>-40°C ≤ TA ≤ +85°C</td>
</tr>
<tr>
<td>D130A</td>
<td>Ed</td>
<td>Cell Endurance</td>
<td>1K</td>
<td>10K</td>
<td>—</td>
<td>E/W</td>
<td>+85°C ≤ TA ≤ +125°C</td>
</tr>
<tr>
<td>D131</td>
<td>VPR</td>
<td>VDD for Read</td>
<td>VMIN</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>VMIN = Minimum operating voltage</td>
</tr>
<tr>
<td>D132</td>
<td>VPEW</td>
<td>VDD for Erase/Write</td>
<td>4.5</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>D133</td>
<td>TPEW</td>
<td>Erase/Write cycle time</td>
<td>—</td>
<td>2</td>
<td>2.5</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>D134</td>
<td>TRET</td>
<td>Characteristic Retention</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>Year</td>
<td>Provided no other specifications are violated</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note**
1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.
2: Negative current is defined as current sourced by the pin.
3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
4: See Section 10.4.1 “Using the Data EEPROM” for additional information.
5: Including OSC2 in CLKOUT mode.
15.6 Thermal Considerations

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Typ</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>TH01</td>
<td>θJA</td>
<td>Thermal Resistance</td>
<td>84.6°C/W</td>
<td>8-pin PDIP package</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Junction to Ambient</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>163.0°C/W</td>
<td>8-pin SOIC package</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>52.4°C/W</td>
<td>8-pin DFN-S 4x4x0.9 mm package</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>46.3°C/W</td>
<td>8-pin DFN-S 6x5 mm package</td>
<td></td>
</tr>
<tr>
<td></td>
<td>θJC</td>
<td>Thermal Resistance</td>
<td>41.2°C/W</td>
<td>8-pin PDIP package</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Junction to Case</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>38.8°C/W</td>
<td>8-pin SOIC package</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.0°C/W</td>
<td>8-pin DFN-S 4x4x0.9 mm package</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.6°C/W</td>
<td>8-pin DFN-S 6x5 mm package</td>
<td></td>
</tr>
<tr>
<td>TH03</td>
<td>TJ</td>
<td>Junction Temperature</td>
<td>150°C</td>
<td></td>
<td>For derated power calculations</td>
</tr>
<tr>
<td>TH04</td>
<td>PD</td>
<td>Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PD = PINTERNAL + PI/O</td>
</tr>
<tr>
<td>TH05</td>
<td>PINTERNAL</td>
<td>Internal Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PINTERNAL = IDD x VDD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(NOTE 1)</td>
</tr>
<tr>
<td>TH06</td>
<td>PI/O</td>
<td>I/O Power Dissipation</td>
<td>—</td>
<td>W</td>
<td>PI/O = Σ(IOL * VOL) + Σ(IOH * (VDD - VOH))</td>
</tr>
<tr>
<td>TH07</td>
<td>PDER</td>
<td>Derated Power</td>
<td>—</td>
<td>W</td>
<td>PDER = (TJ - TA)/θJA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(NOTE 2, 3)</td>
</tr>
</tbody>
</table>

**Note 1:** IDD is current to run the chip alone without driving any load on the output pins.

**Note 2:** TA = Ambient Temperature.

**Note 3:** Maximum allowable power dissipation is the lower value of either the absolute maximum total power dissipation or derated power (PDER).
15.7 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. $T_{ppS}$
2. $T_{pp}$

<table>
<thead>
<tr>
<th>T</th>
<th>Frequency</th>
<th>T</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>cc</td>
<td>osc</td>
<td>OSC1</td>
</tr>
<tr>
<td>F</td>
<td>ck</td>
<td>rd</td>
<td>RD</td>
</tr>
<tr>
<td>F</td>
<td>cs</td>
<td>rw</td>
<td>RD or WR</td>
</tr>
<tr>
<td>F</td>
<td>di</td>
<td>sc</td>
<td>SCK</td>
</tr>
<tr>
<td>F</td>
<td>do</td>
<td>ss</td>
<td>SS</td>
</tr>
<tr>
<td>F</td>
<td>dt</td>
<td>t0</td>
<td>T0CKI</td>
</tr>
<tr>
<td>F</td>
<td>io</td>
<td>t1</td>
<td>T1CKI</td>
</tr>
<tr>
<td>F</td>
<td>mc</td>
<td>wr</td>
<td>WR</td>
</tr>
</tbody>
</table>

Lowercase letters ($pp$) and their meanings:

- cc: CCP1
- ck: CLKOUT
- cs: CS
- di: SDI
- do: SDO
- dt: Data in
- io: I/O PORT
- mc: MCLR

Uppercase letters and their meanings:

- F: Fall
- H: High
- I: Invalid (High-impedance)
- L: Low
- P: Period
- R: Rise
- V: Valid
- Z: High-impedance

FIGURE 15-3: LOAD CONDITIONS

Legend: $CL = 50 \text{ pF}$ for all pins

$CL = 15 \text{ pF}$ for OSC2 output
15.8 AC Characteristics: PIC12F683 (Industrial, Extended)

**TABLE 15-1: CLOCK OSCILLATOR TIMING REQUIREMENTS**

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS01</td>
<td>Fosc</td>
<td>External CLKin Frequency</td>
<td>DC</td>
<td>—</td>
<td>37</td>
<td>kHz</td>
<td>LP Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DC</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td>XT Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DC</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
<td>HS Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DC</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
<td>EC Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Oscillator Frequency</td>
<td>—</td>
<td>32.768</td>
<td>—</td>
<td>kHz</td>
<td>LP Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.1</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td>XT Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>—</td>
<td>20</td>
<td>MHz</td>
<td>HS Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DC</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
<td>RC Oscillator mode</td>
</tr>
<tr>
<td>OS02</td>
<td>Tosc</td>
<td>External CLKin Period</td>
<td>27</td>
<td>—</td>
<td>•</td>
<td>μs</td>
<td>LP Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td>—</td>
<td>•</td>
<td>ns</td>
<td>XT Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>—</td>
<td>•</td>
<td>ns</td>
<td>HS Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>—</td>
<td>•</td>
<td>ns</td>
<td>EC Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Oscillator Period</td>
<td>—</td>
<td>30.5</td>
<td>—</td>
<td>μs</td>
<td>LP Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td>—</td>
<td>10,000</td>
<td>ns</td>
<td>XT Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>—</td>
<td>1,000</td>
<td>ns</td>
<td>HS Oscillator mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>RC Oscillator mode</td>
</tr>
<tr>
<td>OS03</td>
<td>Tcy</td>
<td>Instruction Cycle Time</td>
<td>200</td>
<td>Tcy</td>
<td>DC</td>
<td>ns</td>
<td>Tcy = 4/Fosc</td>
</tr>
<tr>
<td>OS04*</td>
<td>TosH, TosL</td>
<td>External CLKin High, External CLKin Low</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>μs</td>
<td>LP oscillator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>XT oscillator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>HS oscillator</td>
</tr>
<tr>
<td>OS05*</td>
<td>TosR, TosF</td>
<td>External CLKin Rise, External CLKin Fall</td>
<td>0</td>
<td>—</td>
<td>•</td>
<td>ns</td>
<td>LP oscillator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>—</td>
<td>•</td>
<td>ns</td>
<td>XT oscillator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>—</td>
<td>•</td>
<td>ns</td>
<td>HS oscillator</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:**
Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.
### TABLE 15-2: OSCILLATOR PARAMETERS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Freq. Tolerance</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS06</td>
<td>TWARM</td>
<td>Internal Oscillator Switch when running(^{(3)})</td>
<td></td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>Tosc</td>
<td>Slowest clock</td>
</tr>
<tr>
<td>OS07</td>
<td>Tsc</td>
<td>Fail-Safe Sample Clock Period(^{(1)})</td>
<td></td>
<td>—</td>
<td>—</td>
<td>21</td>
<td>ms</td>
<td>LFINTOSC/64</td>
</tr>
<tr>
<td>OS08</td>
<td>HFosc</td>
<td>Internal Calibrated HFINTOSC Frequency(^{(2)})</td>
<td>1%</td>
<td>7.92</td>
<td>8.0</td>
<td>8.08</td>
<td>MHz</td>
<td>VDD = 3.5V, 25°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>±2%</td>
<td>7.84</td>
<td>8.0</td>
<td>8.16</td>
<td>MHz</td>
<td>2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>±5%</td>
<td>7.60</td>
<td>8.0</td>
<td>8.40</td>
<td>MHz</td>
<td>2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.)</td>
</tr>
<tr>
<td>OS09*</td>
<td>LFosc</td>
<td>Internal Uncalibrated LFINTOSC Frequency</td>
<td>—</td>
<td>15</td>
<td>31</td>
<td>45</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>OS10*</td>
<td>Tiosc</td>
<td>HFINTOSC Oscillator Wake-up from Sleep Start-up Time</td>
<td>—</td>
<td>5.5</td>
<td>12</td>
<td>24</td>
<td>μs</td>
<td>VDD = 2.0V, -40°C to +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.5</td>
<td>7</td>
<td>14</td>
<td>μs</td>
<td>VDD = 3.0V, -40°C to +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3</td>
<td>6</td>
<td>11</td>
<td>μs</td>
<td>VDD = 5.0V, -40°C to +85°C</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (Tcy) equals times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

**Note 2:** To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

**Note 3:** By design.
**FIGURE 15-5: CLKOUT AND I/O TIMING**

![CLKOUT and I/O Timing Diagram](image)

**TABLE 15-3: CLKOUT AND I/O TIMING PARAMETERS**

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS11</td>
<td>Tosh2cxl</td>
<td>Fosc↑ to CLKOUT↓ (t&lt;sup&gt;1&lt;/sup&gt;)</td>
<td>—</td>
<td>—</td>
<td>70</td>
<td>ns</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5.0V</td>
</tr>
<tr>
<td>OS12</td>
<td>Tosh2ckh</td>
<td>Fosc↑ to CLKOUT↑ (t&lt;sup&gt;1&lt;/sup&gt;)</td>
<td>—</td>
<td>—</td>
<td>72</td>
<td>ns</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5.0V</td>
</tr>
<tr>
<td>OS13</td>
<td>TckL2ioV</td>
<td>CLKOUT↓ to Port out valid (t&lt;sup&gt;1&lt;/sup&gt;)</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS14</td>
<td>TioV2ckh</td>
<td>Port input valid before CLKOUT↑ (t&lt;sup&gt;1&lt;/sup&gt;)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5.0V</td>
</tr>
<tr>
<td>OS15*</td>
<td>Tosh2ioV</td>
<td>Fosc↑ (Q1 cycle) to Port out valid</td>
<td>50</td>
<td>—</td>
<td>70</td>
<td>ns</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5.0V</td>
</tr>
<tr>
<td>OS16</td>
<td>Tosh2oil</td>
<td>Fosc↑ (Q2 cycle) to Port input invalid</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS17</td>
<td>TioV2osH</td>
<td>Port input valid to Fosc↑ (Q2 cycle)</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>OS18</td>
<td>TioR</td>
<td>Port output rise time (t&lt;sup&gt;2&lt;/sup&gt;)</td>
<td>—</td>
<td>15</td>
<td>72</td>
<td>ns</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 2.0V</td>
</tr>
<tr>
<td>OS19</td>
<td>TioF</td>
<td>Port output fall time (t&lt;sup&gt;2&lt;/sup&gt;)</td>
<td>—</td>
<td>28</td>
<td>55</td>
<td>ns</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 2.0V</td>
</tr>
<tr>
<td>OS20*</td>
<td>Tinp</td>
<td>INT pin input high or low time</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5.0V</td>
</tr>
<tr>
<td>OS21*</td>
<td>Tgpp</td>
<td>GPIO interrupt-on-change new input level time</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated.

**Note 1:** Measurements are taken in RC mode where CLKOUT output is 4 x Tosc.
2: Includes OSC2 in CLKOUT mode.
FIGURE 15-6:
RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

FIGURE 15-7:
BROWN-OUT RESET TIMING AND CHARACTERISTICS

Note 1: Asserted low.

* 64 ms delay only if PWRT is programmed to '0'.

(DEVICE IN BROWN-OUT RESET)

(DEVICE NOT IN BROWN-OUT RESET)
TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated)
Operating Temperature -40°C ≤ TA ≤ +125°C

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>TmCL</td>
<td>MCLR Pulse Width (low)</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>VDD = 5V, -40°C to +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Twdt</td>
<td>Watchdog Timer Time-out</td>
<td>10</td>
<td>16</td>
<td>29</td>
<td>ms</td>
<td>VDD = 5V, -40°C to +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Period (No Prescaler)</td>
<td>10</td>
<td>16</td>
<td>31</td>
<td>ms</td>
<td>VDD = 5V, -40°C to +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VDD = 5V</td>
</tr>
<tr>
<td>32</td>
<td>Tost</td>
<td>Oscillation Start-up Timer</td>
<td>—</td>
<td>1024</td>
<td>—</td>
<td>µs</td>
<td>Tosc (NOTE 3)</td>
</tr>
<tr>
<td>33*</td>
<td>TPWRT</td>
<td>Power-up Timer Period</td>
<td>40</td>
<td>65</td>
<td>140</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>34*</td>
<td>Tioz</td>
<td>I/O High-impedance from MCLR Low or</td>
<td>—</td>
<td>—</td>
<td>2.0</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Watchdog Timer Reset</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>VBor</td>
<td>Brown-out Reset Voltage</td>
<td>2.0</td>
<td>—</td>
<td>2.2</td>
<td>V</td>
<td>(NOTE 4)</td>
</tr>
<tr>
<td>36*</td>
<td>VHyst</td>
<td>Brown-out Reset Hysteresis</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>37*</td>
<td>TBor</td>
<td>Brown-out Reset Minimum Detection</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>VDD ≤ VBOR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Period</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min” values with an external clock input used. The “max” cycle time limit is “DC” (no clock) for all devices.

2: By design.
3: Period of the slower clock.
4: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.
### FIGURE 15-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

![Diagram of Timer0 and Timer1 external clock timings](image)

### TABLE 15-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>40*</td>
<td>T0H</td>
<td>T0CKI High Pulse Width</td>
<td>No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>41*</td>
<td>T0L</td>
<td>T0CKI Low Pulse Width</td>
<td>No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>42*</td>
<td>T0P</td>
<td>T0CKI Period</td>
<td>Greater of:</td>
<td>20 or TCY + 40N</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(N = prescale value (2, 4, ..., 256))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>45*</td>
<td>T1H</td>
<td>T1CKI High Time</td>
<td>Synchronous, No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Synchronous, with Prescaler</td>
<td>15</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Asynchronous</td>
<td>30</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>46*</td>
<td>T1L</td>
<td>T1CKI Low Time</td>
<td>Synchronous, No Prescaler</td>
<td>0.5 TCY + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Synchronous, with Prescaler</td>
<td>15</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Asynchronous</td>
<td>30</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>47*</td>
<td>T1P</td>
<td>T1CKI Input Period</td>
<td>Synchronous</td>
<td>Greater of:</td>
<td>30 or TCY + 40N</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(N = prescale value (1, 2, 4, 8))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>F1</td>
<td>Timer1 Oscillator Input Frequency Range</td>
<td>(oscillator enabled by setting bit T1OSCEN)</td>
<td>—</td>
<td>32.768</td>
<td>—</td>
<td>kHz</td>
</tr>
<tr>
<td>49*</td>
<td>TCKE1</td>
<td>Delay from External Clock Edge to Timer Increment</td>
<td>2 Tosc</td>
<td>—</td>
<td>7 Tosc</td>
<td>—</td>
<td>Timers in Sync mode</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
FIGURE 15-9: CAPTURE/COMPARE/PWM TIMINGS (ECCP)

Note: Refer to Figure 15-3 for load conditions.

TABLE 15-6: CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC01*</td>
<td>TccL</td>
<td>CCP1 Input Low Time</td>
<td>No Prescaler</td>
<td>0.5Tcy + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>CC02*</td>
<td>TccH</td>
<td>CCP1 Input High Time</td>
<td>No Prescaler</td>
<td>0.5Tcy + 20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>With Prescaler</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>CC03*</td>
<td>TccP</td>
<td>CCP1 Input Period</td>
<td></td>
<td>3Tcy + 40/N</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
### TABLE 15-7: COMPARATOR SPECIFICATIONS

#### Standard Operating Conditions (unless otherwise stated)
Operating Temperature: -40°C ≤ TA ≤ +125°C

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristics</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM01</td>
<td>VOS</td>
<td>Input Offset Voltage</td>
<td>—</td>
<td>± 5.0</td>
<td>± 10</td>
<td>mV</td>
<td>(VDD - 1.5)/2</td>
</tr>
<tr>
<td>CM02</td>
<td>VCM</td>
<td>Input Common Mode Voltage</td>
<td>0</td>
<td>—</td>
<td>VDD - 1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CM03*</td>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>+55</td>
<td>—</td>
<td>—</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>CM04*</td>
<td>TRT</td>
<td>Response Time</td>
<td>Falling</td>
<td>—</td>
<td>150</td>
<td>600</td>
<td>ns (NOTE 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Rising</td>
<td>—</td>
<td>200</td>
<td>1000</td>
<td>ns</td>
</tr>
<tr>
<td>CM05*</td>
<td>TMC2COV</td>
<td>Comparator Mode Change to</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>μs</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Response time is measured with one comparator input at (VDD - 1.5)/2 - 100 mV to (VDD - 1.5)/2 + 20 mV.

### TABLE 15-8: COMPARATOR VOLTAGE REFERENCE (CVRREF) SPECIFICATIONS

#### Standard Operating Conditions (unless otherwise stated)
Operating temperature: -40°C ≤ TA ≤ +125°C

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristics</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV01*</td>
<td>CLSB</td>
<td>Step Size(2)</td>
<td>—</td>
<td>—</td>
<td>VDD/24</td>
<td>V</td>
<td>Low Range (VRR = 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VDD/32</td>
<td>V</td>
<td>High Range (VRR = 0)</td>
</tr>
<tr>
<td>CV02*</td>
<td>CACC</td>
<td>Absolute Accuracy</td>
<td>—</td>
<td>—</td>
<td>± 1/2</td>
<td>LSb</td>
<td>Low Range (VRR = 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1/2</td>
<td>LSb</td>
<td>High Range (VRR = 0)</td>
</tr>
<tr>
<td>CV03*</td>
<td>CR</td>
<td>Unit Resistor Value (R)</td>
<td>—</td>
<td>2k</td>
<td>—</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>CV04*</td>
<td>CST</td>
<td>Settling Time(1)</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>μs</td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

**Note 2:** See Section 8.11 “Comparator Voltage Reference” for more information.
### TABLE 15-9: PIC12F683 A/D CONVERTER (ADC) CHARACTERISTICS

**Standard Operating Conditions (unless otherwise stated)**

Operating temperature $-40^\circ\text{C} \leq TA \leq +125^\circ\text{C}$

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD01</td>
<td>NR</td>
<td>Resolution</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>bits</td>
<td></td>
</tr>
<tr>
<td>AD02</td>
<td>EIL</td>
<td>Integral Error</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>LSB</td>
<td>VREF = 5.12V</td>
</tr>
<tr>
<td>AD03</td>
<td>EDL</td>
<td>Differential Error</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>LSB</td>
<td>No missing codes to 10 bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VREF = 5.12V</td>
</tr>
<tr>
<td>AD04</td>
<td>EOFF</td>
<td>Offset Error</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>LSB</td>
<td>VREF = 5.12V</td>
</tr>
<tr>
<td>AD07</td>
<td>EGN</td>
<td>Gain Error</td>
<td>—</td>
<td>—</td>
<td>±1</td>
<td>LSB</td>
<td>VREF = 5.12V</td>
</tr>
<tr>
<td>AD06</td>
<td>VREF</td>
<td>Reference Voltage$^{(3)}$</td>
<td>2.2</td>
<td>—</td>
<td>—</td>
<td>VDD</td>
<td>Absolute minimum to ensure 1 LSB accuracy</td>
</tr>
<tr>
<td>AD06A</td>
<td></td>
<td></td>
<td>2.7</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AD07</td>
<td>VAIN</td>
<td>Full-Scale Range</td>
<td>VSS</td>
<td>—</td>
<td>VREF</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>AD08</td>
<td>ZAIN</td>
<td>Recommended Impedance of Analog Voltage Source</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>AD09*</td>
<td>IREF</td>
<td>VREF Input Current$^{(3)}$</td>
<td>10</td>
<td>—</td>
<td>1000</td>
<td>μA</td>
<td>During VAIN acquisition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Based on differential of VHOLD to VAIN.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note**

1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: ADC VREF is from external VREF or VDD pin, whichever is selected as reference input.

4: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.
## TABLE 15-10: PIC12F683 A/D CONVERSION REQUIREMENTS

### Standard Operating Conditions (unless otherwise stated)

- Operating temperature: $-40°C \leq T_A \leq +125°C$

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Sym</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD130*</td>
<td>TAD</td>
<td>A/D Clock Period</td>
<td>1.6</td>
<td>—</td>
<td>9.0</td>
<td>μs</td>
<td>TOSC-based, $V_{REF \geq 3.0V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A/D Internal RC Oscillator Period</td>
<td>3.0</td>
<td>—</td>
<td>9.0</td>
<td>μs</td>
<td>TOSC-based, $V_{REF full range}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.0</td>
<td>6.0</td>
<td>9.0</td>
<td>μs</td>
<td>$ADCS&lt;1:0&gt; = 11$ (ADRC mode)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.6</td>
<td>4.0</td>
<td>6.0</td>
<td>μs</td>
<td>At $V_{DD} = 2.5V$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>At $V_{DD} = 5.0V$</td>
</tr>
<tr>
<td>AD131</td>
<td>TCNV</td>
<td>Conversion Time (not including</td>
<td>—</td>
<td>11</td>
<td>—</td>
<td>TAD</td>
<td>Set GO/DONE bit to new data in A/D</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Acquisition Time)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Result register.</td>
</tr>
<tr>
<td>AD132*</td>
<td>TACQ</td>
<td>Acquisition Time</td>
<td></td>
<td>11.5</td>
<td>—</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>AD133*</td>
<td>TAMP</td>
<td>Amplifier Settling Time</td>
<td></td>
<td>—</td>
<td>5</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>AD134</td>
<td>TGO</td>
<td>Q4 to A/D Clock Start</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.
† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** ADRESH and ADRESL registers may be read on the following TCY cycle.

**Note 2:** See Section 9.3 “A/D Acquisition Requirements” for minimum conditions.
FIGURE 15-10: PIC12F683 A/D CONVERSION TIMING (NORMAL MODE)

![Diagram of A/D conversion timing for normal mode]

Note 1: If the A/D clock source is selected as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

FIGURE 15-11: PIC12F683 A/D CONVERSION TIMING (SLEEP MODE)

![Diagram of A/D conversion timing for sleep mode]

Note 1: If the A/D clock source is selected as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables, the data presented are outside specified operating range (i.e., outside specified VDD range). This is for information only and devices are ensured to operate properly only within the specified range.

| Note: | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range. |

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 16-1: TYPICAL IDD VS. FOSC OVER VDD (EC MODE)

![Graph showing typical IDD vs. FOSC over VDD (EC mode)]
FIGURE 16-2: MAXIMUM IDD vs. FOSC OVER VDD (EC MODE)

![Graph showing the relationship between IDD and FOSC over VDD for EC mode.](image1)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)

FIGURE 16-3: TYPICAL IDD vs. FOSC OVER VDD (HS MODE)

![Graph showing the relationship between IDD and FOSC over VDD for HS mode.](image2)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)
FIGURE 16-4: MAXIMUM \( \text{IDD} \) vs. \( \text{FOSC} \) OVER \( \text{VDD} \) (HS MODE)

![Graph showing \( \text{MAXIMUM \( \text{IDD} \)} \) vs. \( \text{FOSC} \) OVER \( \text{VDD} \) (HS MODE)]

FIGURE 16-5: TYPICAL \( \text{IDD} \) vs. \( \text{VDD} \) OVER \( \text{FOSC} \) (XT MODE)

![Graph showing \( \text{TYPICAL \( \text{IDD} \)} \) vs. \( \text{VDD} \) OVER \( \text{FOSC} \) (XT MODE)]
FIGURE 16-6: MAXIMUM IDD vs. VDD OVER FOSC (XT MODE)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)

VDD (V)

IDD (μA)

VDD (V)

IDD (μA)

FIGURE 16-7: TYPICAL IDD vs. VDD OVER FOSC (EXTRC MODE)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)

VDD (V)

IDD (μA)

VDD (V)

IDD (μA)
FIGURE 16-8: MAXIMUM IDD vs. VDD (EXTRC MODE)

FIGURE 16-9: IDD vs. VDD OVER FOSC (LFINTOSC MODE, 31 kHz)
FIGURE 16-10: $I_{DD}$ vs. $V_{DD}$ (LP MODE)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)

32 kHz Maximum

$V_{DD}$ (V)

$I_{DD}$ (μA)

2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5

FIGURE 16-11: TYPICAL $I_{DD}$ vs. FOSC OVER $V_{DD}$ (HFINTOSC MODE)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)

32 kHz Maximum

$V_{DD}$ (V)

$I_{DD}$ (μA)

2.0V 3.0V 4.0V 5.0V 5.5V

0 200 400 600 800 1,000 1,200 1,400 1,600

125 kHz 250 kHz 500 kHz 1 MHz 2 MHz 4 MHz 8 MHz

FOSC
FIGURE 16-12:  MAXIMUM IDD vs. FOSC OVER VDD (HFINTOSC MODE)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)

FIGURE 16-13:  TYPICAL IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)
FIGURE 16-14: MAXIMUM IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)

![Graph showing Maximum IPD vs. VDD for SLEEP MODE with all peripherals disabled.]

Maximum: Mean + 3σ (Worst-case Temp) (-40°C to 125°C)
Max. 125°C
Max. 85°C

FIGURE 16-15: COMPARATOR IPD vs. VDD (BOTH COMPARATORS ENABLED)

![Graph showing COMPARATOR IPD vs. VDD for both comparators enabled.]

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ (-40°C to 125°C)
Maximum
Typical
FIGURE 16-16: BOR \( I_{PD} \) vs. \( V_{DD} \) OVER TEMPERATURE

- Typical: Statistical Mean @25°C
- Maximum: Mean (Worst-case Temp) + 3σ
  (-40°C to 125°C)

FIGURE 16-17: TYPICAL WDT \( I_{PD} \) vs. \( V_{DD} \) OVER TEMPERATURE

- Typical: Statistical Mean @25°C
- Maximum: Mean (Worst-case Temp) + 3σ
  (-40°C to 125°C)
FIGURE 16-18: MAXIMUM WDT IPD vs. VDD OVER TEMPERATURE

FIGURE 16-19: WDT PERIOD vs. VDD OVER TEMPERATURE
FIGURE 16-20: WDT PERIOD vs. TEMPERATURE OVER VDD (5.0V)

FIGURE 16-21: CVREF IPD vs. VDD OVER TEMPERATURE (HIGH RANGE)
FIGURE 16-22: CVREF IPD vs. VDD OVER TEMPERATURE (LOW RANGE)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)

FIGURE 16-23: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)
**FIGURE 16-24: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)**

![VOL vs. IOL Over Temperature](image)

- Typical: Statistical Mean @25°C
- Maximum: Mean (Worst-case Temp) + 3σ (-40°C to 125°C)

**FIGURE 16-25: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)**

![VOH vs. IOH Over Temperature](image)

- Typical: Statistical Mean @25°C
- Maximum: Mean (Worst-case Temp) + 3σ (-40°C to 125°C)
FIGURE 16-26: $V_{OH}$ vs. $I_{OH}$ OVER TEMPERATURE ($V_{DD} = 5.0V$)

![Graph showing $V_{OH}$ vs. $I_{OH}$ over temperature with different curves for max, typ, and min conditions at -40°C to 125°C.]

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ (-40°C to 125°C)

FIGURE 16-27: TTL INPUT THRESHOLD $V_{IN}$ vs. $V_{DD}$ OVER TEMPERATURE

![Graph showing $V_{IN}$ vs. $V_{DD}$ over temperature with different curves for max, typ, and min conditions at -40°C to 125°C.]

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ (-40°C to 125°C)
FIGURE 16-28: SCHMITT TRIGGER INPUT THRESHOLD $V_{IN}$ vs. $V_{DD}$ OVER TEMPERATURE

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)

FIGURE 16-29: T1OSC $I_{PD}$ vs. $V_{DD}$ OVER TEMPERATURE (32 kHz)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)
FIGURE 16-30: COMPARATOR RESPONSE TIME (RISING EDGE)

Note:
- VCM = VDD - 1.5V/2
- V- input = Transition from VCM + 100mV to VCM - 20mV

FIGURE 16-31: COMPARATOR RESPONSE TIME (FALLING EDGE)

Note:
- VCM = VDD - 1.5V/2
- V+ input = VCM
- V- input = Transition from VCM - 100mV to VCM + 20mV
FIGURE 16-32: LFINTOSC FREQUENCY vs. VDD OVER TEMPERATURE (31 kHz)

Typical: Statistical Mean @25°C
Maximum: Mean (Worst-case Temp) + 3σ
(-40°C to 125°C)

FIGURE 16-33: ADC CLOCK PERIOD vs. VDD OVER TEMPERATURE
FIGURE 16-34: TYPICAL HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

FIGURE 16-35: MAXIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE
**FIGURE 16-36: MINIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE**

![Minimum HFINTOSC Start-up Times vs. VDD Over Temperature](image)

- Typical: Statistical Mean @25°C
- Maximum: Mean (Worst-case Temp) + 3σ (-40°C to 125°C)

**FIGURE 16-37: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (25°C)**

![Typical HFINTOSC Frequency Change vs. VDD (25°C)](image)
FIGURE 16-38: TYPICAL HFINTOSC FREQUENCY CHANGE OVER DEVICE VDD (85°C)

FIGURE 16-39: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (125°C)
FIGURE 16-40: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (-40°C)
17.0 PACKAGING INFORMATION

17.1 Package Marking Information

8-Lead PDIP

Example

\[
\begin{array}{c}
\text{XXXXXXX} \\
\text{XXXXXNNN} \\
\text{YYWW} \\
\end{array}
\]

12F683
I/P \(\varepsilon^3\) 017
O \(\varepsilon^3\) 0415

8-Lead SOIC (3.90 mm)

Example

\[
\begin{array}{c}
\text{XXXXXXX} \\
\text{XXXXYWW} \\
\text{NNN} \\
\end{array}
\]

12F683 \(\varepsilon^3\)
I/SN0415
O \(\varepsilon^3\) 017

8-Lead DFN (4x4x0.9 mm)

Example

\[
\begin{array}{c}
\text{XXXXXXX} \\
\text{YYYYYY} \\
\text{YYWW} \\
\text{NNN} \\
\end{array}
\]

12F683
I/MD \(\varepsilon^3\)
0415
O \(\varepsilon^3\) 017

8-Lead DFN-S (6x5 mm)

Example

\[
\begin{array}{c}
\text{XXXXXXX} \\
\text{XXXXXX} \\
\text{XXYYWW} \\
\text{NNN} \\
\end{array}
\]

12F683
I/MF \(\varepsilon^3\)
0415
O \(\varepsilon^3\) 017

Legend:  
XX...X  Customer-specific information  
Y  Year code (last digit of calendar year)  
YY  Year code (last 2 digits of calendar year)  
WW  Week code (week of January 1 is week ‘01’)  
NNN  Alphanumeric traceability code  
\(\varepsilon^3\)  Pb-free JEDEC designator for Matte Tin (Sn)  
*  This package is Pb-free. The Pb-free JEDEC designator \(\varepsilon^3\) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard PIC® device marking consists of Microchip part number, year code, week code and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.
17.2 Package Details

The following sections give the technical details of the packages.

8-Lead Plastic Dual In-Line (P or PA) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

### Notes:
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

---

<table>
<thead>
<tr>
<th>Units</th>
<th>INCHES</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td>.100 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Top to Seating Plane</td>
<td>A</td>
<td>–</td>
<td>–</td>
<td>.210</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>.115</td>
<td>.130</td>
<td>.195</td>
</tr>
<tr>
<td>Base to Seating Plane</td>
<td>A1</td>
<td>.015</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Shoulder to Shoulder Width</td>
<td>E</td>
<td>.290</td>
<td>.310</td>
<td>.325</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>.240</td>
<td>.250</td>
<td>.280</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>.348</td>
<td>.365</td>
<td>.400</td>
</tr>
<tr>
<td>Tip to Seating Plane</td>
<td>L</td>
<td>.115</td>
<td>.130</td>
<td>.150</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
<td>.008</td>
<td>.010</td>
<td>.015</td>
</tr>
<tr>
<td>Upper Lead Width</td>
<td>b1</td>
<td>.040</td>
<td>.060</td>
<td>.070</td>
</tr>
<tr>
<td>Lower Lead Width</td>
<td>b</td>
<td>.014</td>
<td>.018</td>
<td>.022</td>
</tr>
<tr>
<td>Overall Row Spacing §</td>
<td>eB</td>
<td>–</td>
<td>–</td>
<td>.430</td>
</tr>
</tbody>
</table>

---

Microchip Technology Drawing C04-018
8-Lead Plastic Small Outline (SN or OA) – Narrow, 3.90 mm Body [SOIC]

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

---

**Units** | **MILLIMETERS**
--- | ---
| **Dimension Limits** | **MIN** | **NOM** | **MAX**
--- | --- | --- | ---
Number of Pins | N | 8 |
Pitch | e | 1.27 BSC |
Overall Height | A | – | – | 1.75 |
Molded Package Thickness | A2 | 1.25 | – | – |
Standoff § | A1 | 0.10 | – | 0.25 |
Overall Width | E | 6.00 BSC |
Molded Package Width | E1 | 3.90 BSC |
Overall Length | D | 4.90 BSC |
Chamfer (optional) | h | 0.25 | – | 0.50 |
Foot Length | L | 0.40 | – | 1.27 |
Footprint | L1 | 1.04 REF |
Foot Angle | φ | 0° | – | 8° |
Lead Thickness | c | 0.17 | – | 0.25 |
Lead Width | b | 0.31 | – | 0.51 |
Mold Draft Angle Top | α | 5° | – | 15° |
Mold Draft Angle Bottom | β | 5° | – | 15° |
8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Contact Thickness</td>
<td>A3</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
</tr>
<tr>
<td>Contact Width</td>
<td>b</td>
</tr>
<tr>
<td>Contact Length</td>
<td>L</td>
</tr>
<tr>
<td>Contact-to-Exposed Pad</td>
<td>K</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131C
8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Dimensioning and tolerancing per ASME Y14.5M.

**Units MILLIMETERS**

<table>
<thead>
<tr>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td>1.27 BSC</td>
<td></td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
<td>–</td>
<td>0.85</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>–</td>
<td>0.65</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
<td>0.00</td>
<td>0.01</td>
</tr>
<tr>
<td>Base Thickness</td>
<td>A3</td>
<td>0.20 REF</td>
<td></td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td>4.92 BSC</td>
<td></td>
</tr>
<tr>
<td>Molded Package Length</td>
<td>D1</td>
<td>4.67 BSC</td>
<td></td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
<td>3.85</td>
<td>4.00</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
<td>5.99 BSC</td>
<td></td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td>5.74 BSC</td>
<td></td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
<td>2.16</td>
<td>2.31</td>
</tr>
<tr>
<td>Contact Width</td>
<td>b</td>
<td>0.35</td>
<td>0.40</td>
</tr>
<tr>
<td>Contact Length</td>
<td>L</td>
<td>0.50</td>
<td>0.60</td>
</tr>
<tr>
<td>Contact-to-Exposed Pad</td>
<td>K</td>
<td>0.20</td>
<td>–</td>
</tr>
<tr>
<td>Model Draft Angle Top</td>
<td></td>
<td>0.20</td>
<td>–</td>
</tr>
</tbody>
</table>

**Notes:**
- For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
APPENDIX A: DATA SHEET

Revision A
This is a new data sheet.

Revision B
Rewrites of the Oscillator and Special Features of the CPU sections. General corrections to Figures and formatting.

Revision C
Revisions throughout document. Incorporated Golden Chapters.

Revision D
Replaced Package Drawings; Revised Product ID Section (SN package to 3.90 mm); Replaced PICmicro with PIC; Replaced Dev Tool Section.

APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from other PIC devices to the PIC12F683 device.

B.1 PIC16F676 to PIC12F683

TABLE B-1: FEATURE COMPARISON

<table>
<thead>
<tr>
<th>Feature</th>
<th>PIC16F676</th>
<th>PIC12F683</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Operating Speed</td>
<td>20 MHz</td>
<td>20 MHz</td>
</tr>
<tr>
<td>Max Program Memory (Words)</td>
<td>1024</td>
<td>2048</td>
</tr>
<tr>
<td>SRAM (bytes)</td>
<td>64</td>
<td>128</td>
</tr>
<tr>
<td>A/D Resolution</td>
<td>10-bit</td>
<td>10-bit</td>
</tr>
<tr>
<td>Data EEPROM (Bytes)</td>
<td>128</td>
<td>256</td>
</tr>
<tr>
<td>Timers (8/16-bit)</td>
<td>1/1</td>
<td>2/1</td>
</tr>
<tr>
<td>Oscillator Modes</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Brown-out Reset</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Internal Pull-ups</td>
<td>RA0/1/2/4/5</td>
<td>GP0/1/2/4/5, MCLR</td>
</tr>
<tr>
<td>Interrupt-on-change</td>
<td>RA0/1/2/3/4/5</td>
<td>GP0/1/2/3/4/5</td>
</tr>
<tr>
<td>Comparator</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>ECCP</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>Ultra Low-Power Wake-Up</td>
<td>N</td>
<td>Y</td>
</tr>
<tr>
<td>Extended WDT</td>
<td>N</td>
<td>Y</td>
</tr>
<tr>
<td>Software Control Option of WDT/BOR</td>
<td>N</td>
<td>Y</td>
</tr>
<tr>
<td>INTOSC Frequencies</td>
<td>4 MHz</td>
<td>32 kHz-8 MHz</td>
</tr>
<tr>
<td>Clock Switching</td>
<td>N</td>
<td>Y</td>
</tr>
</tbody>
</table>

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.
INDEX

A
A/D
Specifications................................................................. 133, 134
Absolute Maximum Ratings .................................................. 115
AC Characteristics
Industrial and Extended ......................................................... 125
Load Conditions ........................................................................ 124
ADC .......................................................................................... 61
Acquisition Requirements ......................................................... 67
Associated registers ............................................................. 69
Block Diagram ........................................................................ 61
Calculating Acquisition Time ................................................ 67
Channel Selection ..................................................................... 61
Configuration ........................................................................... 61
Configuring Interrupt .................................................................. 64
Conversion Clock ..................................................................... 62
Conversion Procedure ................................................................ 64
GPIO Configuration .................................................................. 61
Internal Sampling Switch (RSS) IMPEDANCE .............................. 67
Interrupts .................................................................................. 63
Operation .................................................................................. 63
Operation During Sleep ............................................................ 64
Reference Voltage (VREF) .................................................... 62
Result Formatting ...................................................................... 63
Source Impedance ..................................................................... 67
Special Event Trigger .............................................................. 64
Starting an A/D Conversion ..................................................... 63
ADCON0 Register ..................................................................... 65
ADRES Register (ADFM = 0) .................................................. 66
ADRES Register (ADFM = 1) .................................................. 66
ADRESL Register (ADFM = 0) .................................................. 66
ADRESL Register (ADFM = 1) .................................................. 66
Analog Input Connection Considerations .................................... 52
Analog-to-Digital Converter. See ADC ......................................... 69
ANSEL Register ....................................................................... 33
Assembler
MPASM Assembler .................................................................. 112

B
Block Diagrams
(CCP) Capture Mode Operation ........................................... 76
ADC ......................................................................................... 61
ADC Transfer Function .......................................................... 68
Analog Input Model ............................................................... 52, 68
CCP PWM................................................................................. 78
Clock Source ............................................................................ 19
Comparator ............................................................................... 51
Compare ................................................................................... 77
Crystal Operation ....................................................................... 22
External RC Mode ..................................................................... 23
Fail-Safe Clock Monitor (FSCM) ................................................ 29
GP1 Pin ...................................................................................... 37
GP2 Pin ...................................................................................... 37
GP3 Pin ...................................................................................... 38
GP4 Pin ...................................................................................... 38
GP5 Pin ...................................................................................... 39
In-Circuit Serial Programming Connections .............................. 100
Interrupt Logic .......................................................................... 93
MCLR Circuit ............................................................................. 86
On-Chip Reset Circuit .............................................................. 85
PIC12F683 .................................................................................. 9
Resonator Operation ................................................................. 22
Timer1 ....................................................................................... 44

C
C Compilers
MPLAB C18 ............................................................................. 112
MPLAB C30 ............................................................................. 112
Calibration Bits ......................................................................... 85
Capture Module. See Capture/Compare/PWM (CCP) ..... 75
Capture/Compare/PWM (CCP) .................................................. 75
Associated registers w/ Capture, Compare and Timer1 .................. 81
Associated registers w/ PWM and Compare ................................. 81
Capture Mode ........................................................................... 76
CCPx Pin Configuration ............................................................ 76
Compare Mode ........................................................................... 77
CCPx Pin Configuration ............................................................ 77
Software Interrupt Mode .......................................................... 76, 77
Special Event Trigger ............................................................... 77
Timer1 Mode Selection ............................................................. 76, 77
Prewcaler .................................................................................. 76
PWM Mode ................................................................................. 78
Duty Cycle ............................................................................... 79
Effects of Reset ......................................................................... 80
Example PWM Frequencies and Resolutions, 20 MHZ .............. 79
Example PWM Frequencies and Resolutions, 8 MHZ .............. 79
Operation in Sleep Mode ........................................................... 80
Setup for Operation ................................................................. 80
System Clock Frequency Changes .............................................. 80
PWM Period ............................................................................... 79
Setup for PWM Operation ......................................................... 80
Timer Resources ......................................................................... 75
CCP. See Capture/Compare/PWM (CCP) ................................. 75
CCP1CON Register ................................................................. 75
Clock Sources
External Modes ......................................................................... 21
EC ......................................................................................... 21
HS ......................................................................................... 22
LP ......................................................................................... 22
OST ....................................................................................... 21
RC ......................................................................................... 23
XT ......................................................................................... 22
Internal Modes .......................................................................... 23
Frequency Selection ............................................................... 25
HFINTOSC ............................................................................... 23
INTOSC .................................................................................. 23
INTOSCI .................................................................................. 23
LFINTOSC ............................................................................... 25
Clock Switching .......................................................................... 27
Code Examples
A/D Conversion ......................................................................... 64
Assigning Prescaler to Timer0 .................................................. 42
Assigning Prescaler to WDT ..................................................... 42
 Changing Between Capture Prescalers ........................................ 76
Data EEPROM Read ............................................................... 73
Data EEPROM Write ............................................................... 73

© 2007 Microchip Technology Inc.
PIC12F683

Indirect Addressing ................................................. 18
Initializing GPIO .......................................................... 31
Saving STATUS and W Registers in RAM.................. 95
Ultra Low-Power Wake-up Initialization ......... 35
Write Verify .............................................................. 73
Code Protection .......................................................... 99
Comparator ................................................................. 51
C2OUT as T1 Gate ......................................................... 57
Configurations ............................................................. 53
I/O Operating Modes .................................................. 53
Interrupts ................................................................. 55
Operation ................................................................. 51, 54
Operation During Sleep ......................................... 56
Response Time .......................................................... 54
Synchronizing COUT w/Timer1 ................................ 57
Comparator Module
Associated registers .................................................. 59
 Comparator Voltage Reference (CVREF)
Response Time .......................................................... 54
 Comparator Voltage Reference (CVREF) ................. 58
Effects of a Reset ....................................................... 56
Specifications .......................................................... 132
Comparators
C2OUT as T1 Gate ......................................................... 45
Effects of a Reset ....................................................... 56
Specifications .......................................................... 132
Compare Module. See Capture/Compare/PWM (CCP)
CONFIG Register ........................................................ 84
Configuration Bits ...................................................... 83
CPU Features .......................................................... 83
Customer Change Notification Service .......... 171
Customer Notification Service ...................... 171
Customer Support .................................................... 171
D
Data EEPROM Memory
Associated Registers .................................................. 74
Code Protection ........................................................ 71, 74
Data Memory Organization ...................................... 7
Map of the PIC12F683 ................................................. 8
DC and AC Characteristics
Graphs and Tables ..................................................... 137
DC Characteristics
Extended and Industrial ........................................ 121
Industrial and Extended ....................................... 117
Development Support ............................................. 111
Device Overview ...................................................... 5
E
EEADR Register .......................................................... 71
EECON1 Register ....................................................... 72
EECON2 Register ....................................................... 72
EEDAT Register .......................................................... 71
EE PROM Data Memory
Avoiding Spurious Write ....................................... 74
Reading ................................................................. 73
Write Verify ............................................................ 73
Writing ................................................................. 73
Effects of Reset
PWM mode ........................................................... 80
Electrical Specifications ............................................... 115
Enhanced Capture/Compare/PWM (ECCP)
Specifications ......................................................... 131
Errata ................................................................... 3

F
Fail-Safe Clock Monitor ............................................... 29
Fail-Safe Condition Clearing ................................... 29
Fail-Safe Detection ................................................... 29
Fail-Safe Operation ................................................... 29
Reset or Wake-up from Sleep ................................ 29
Firmware Instructions ............................................... 101
Fuses. See Configuration Bits

G
General Purpose Register File ..................................... 8
GPIO ....................................................................... 31
Additional Pin Functions ........................................... 32
ANSEL Register ......................................................... 32
Interrupt-on-Change ............................................... 32
Ultra Low-Power Wake-up ..................................... 32, 35
Weak Pull-up ............................................................ 32
Associated Registers ................................................ 39
GP0 ................................................................. 36
GP1 ................................................................. 37
GP2 ................................................................. 37
GP3 ................................................................. 38
GP4 ................................................................. 38
GP5 ................................................................. 39
Pin Descriptions and Diagrams ................................ 36
Specifications ........................................................ 127
GPIO Register .......................................................... 31

I
ID Locations ............................................................ 99
In-Circuit Debugger ................................................... 100
In-Circuit Serial Programming (ICSP) ................. 100
Indirect Addressing, INDF and FSR Registers .... 18
Instruction Format ..................................................... 101
Instruction Set ......................................................... 101
ADD LW .............................................................. 103
ADD W .............................................................. 103
AND LW .............................................................. 103
AND W .............................................................. 103
BCF ................................................................. 103
BSF ................................................................. 103
BT FSC .............................................................. 103
BT FSS .............................................................. 104
CALL ............................................................... 104
CLR F .............................................................. 104
CLR W .............................................................. 104
CLR WDT ............................................................ 104
COM F .............................................................. 104
DECF .............................................................. 104
DEC FSZ ........................................................... 105
GOTO ............................................................... 105
INCF ............................................................... 105
INCFS Z ........................................................... 105
IOR LW .............................................................. 105
IOR WF ............................................................ 105
MOV F ............................................................ 106
MOV LW ........................................................... 106
MOV W ............................................................ 106
NOP ................................................................. 106
RETF IE ........................................................... 107
RETL W ............................................................ 107
RETURN .......................................................... 107
RLF ................................................................. 108
RRF ................................................................. 108
SLEEP ............................................................... 108

DS41211D-page 168 © 2007 Microchip Technology Inc.
PIC12F683

WDTCON (Watchdog Timer Control) ........................................ 97
WPU (Weak Pull-Up GPIO) ......................................................... 34
Resets .................................................................................. 85
Brown-out Reset (BOR) ......................................................... 85
MCLR Reset, Normal Operation ............................................. 85
MCLR Reset, Sleep .................................................................. 85
Power-on Reset (POR) ........................................................... 85
WDT Reset, Normal Operation ............................................. 85
WDT Reset, Sleep .................................................................. 85
Revision History .................................................................. 165

S
Sleep
Power-Down Mode ............................................................... 98
Wake-up ............................................................................... 98
Wake-up Using Interrupts .................................................. 98
Software Simulator (MPLAB SIM) ........................................ 112
Special Event Trigger .......................................................... 64
Special Function Registers .................................................... 8
STATUS Register .................................................................. 12

T
T1CON Register .................................................................. 47
T2CON Register .................................................................. 50
Thermal Considerations ...................................................... 123
Time-out Sequence ............................................................ 88
Timer0 ................................................................................. 41
Associated Registers .......................................................... 43
External Clock ..................................................................... 42
Interrupt ............................................................................ 41, 43
Operation .............................................................................. 41, 44
Specifications ....................................................................... 130
TOCKI.................................................................................. 42
Timer1 .................................................................................. 44
Associated registers ............................................................. 48
Asynchronous Counter Mode ............................................. 45
Reading and Writing ............................................................ 45
Interrupt ................................................................................. 46
Modes of Operation ............................................................ 44
Operation During Sleep ....................................................... 46
Oscillator ............................................................................ 45
Prescaler .............................................................................. 45
Specifications ......................................................................... 130
Timer1 Gate
Inverting Gate ..................................................................... 45
Selecting Source ................................................................. 45, 57
Synchronizing COUT w/Timer1 ......................................... 57
TMR1H Register .................................................................. 44
TMR1L Register .................................................................. 44
Timer2
Associated registers ............................................................. 50
Timers
Timer1
T1CON .................................................................................. 47
Timer2
T2CON .................................................................................. 50
Timing Diagrams
A/D Conversion ................................................................. 135
A/D Conversion (Sleep Mode) ............................................. 135
Brown-out Reset (BOR) ....................................................... 128
Brown-out Reset Situations ............................................. 87
CLKOUT and I/O ............................................................... 127
Clock Timing ..................................................................... 125
Comparator Output ............................................................ 51
Enhanced Capture/Compare/PWM (ECCP) ..................... 131
Fail-Safe Clock Monitor (FSCM) ....................................... 30
INT Pin Interrupt ................................................................. 94
Internal Oscillator Switch Timing ....................................... 26
Reset, WDT, OST and Power-up Timer ......................... 128
Time-out Sequence on Power-up (Delayed MCLR) ........ 89
Time-out Sequence on Power-up (MCLR with VDD) ....... 89
Timer0 and Timer1 External Clock .................................. 130
Timer1 Incrementing Edge ............................................... 46
Two Speed Start-up .............................................................. 28
Wake-up from Sleep Through Interrupt ......................... 99
Timing Parameter Symbology ........................................... 124
TRISIO Register ................................................................. 32
Two-Speed Clock Start-up Mode ..................................... 27

U
Ultra Low-Power Wake-up .............................................. 32, 35

V
Voltage Reference. See Comparator Voltage
Reference (CVREF)
Voltage References
Associated registers .......................................................... 59
VREF. See ADC Reference Voltage

W
Wake-up Using Interrupts .................................................... 98
Watchdog Timer (WDT) ........................................................ 96
Associated Registers .......................................................... 97
Clock Source ..................................................................... 96
Modes ................................................................................. 96
Period ................................................................................. 96
Specifications ....................................................................... 129
WDTCON Register ............................................................. 97
WPU Register ..................................................................... 34
WWW Address ..................................................................... 171
WWW. On-Line Support .................................................. 3
THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user’s guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip’s customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com
READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager Total Pages Sent ________
RE: Reader Response

From: Name ________________________________
Company ________________________________
Address ________________________________
City / State / ZIP / Country ________________
Telephone: (______) _________ - _________ FAX: (______) _________ - _________

Application (optional):

Would you like a reply? Y N

Device: PIC12F683 Literature Number: DS41211D

Questions:
1. What are the best features of this document?

__________________________________________________________________________

2. How does this document meet your hardware and software development needs?

__________________________________________________________________________

3. Do you find the organization of this document easy to follow? If not, why?

__________________________________________________________________________

4. What additions to the document do you think would enhance the structure and subject?

__________________________________________________________________________

5. What deletions from the document could be made without affecting the overall usefulness?

__________________________________________________________________________

6. Is there any incorrect or misleading information (what and where)?

__________________________________________________________________________

7. How would you improve this document?

__________________________________________________________________________
PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X</th>
<th>XX</th>
<th>XXX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>Temperature</td>
<td>Package</td>
<td>Pattern</td>
</tr>
</tbody>
</table>

Device: PIC12F683(1), PIC12F683T(2)
VDD range 2.0V to 5.5V

Temperature Range:
- I = -40°C to +85°C (Industrial)
- E = -40°C to +125°C (Extended)

Package:
- P = Plastic DIP
- MD = Dual-Flat, No Leads (DFN-S, 4x4x0.9 mm)
- MF = Dual-Flat, No Leads (DFN-S, 6x5 mm)
- SN = 8-lead Small Outline (3.90 mm)

Pattern:
3-digit Pattern Code for QTP (blank otherwise)

Examples:
- a) PIC12F683-E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301
- b) PIC12F683-I/SN = Industrial Temp., SOIC package, 20 MHz

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range
2: T = in tape and reel PLCC, and TQFP packages only.