LF147/LF347 Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description
The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (Bi-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features
- Internally trimmed offset voltage 5 mV max
- Low input bias current 50 pA
- Low input noise current 0.01 pA/√Hz
- Wide gain bandwidth 4 MHz
- High slew rate 13 V/μs
- Low supply current 7.2 mA
- High input impedance 10¹²X
- Low total harmonic distortion A_Ve 10, A_RL 10k, V_O 20 Vp-p, BW 20 Hz - 20 kHz
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

Simplified Schematic

Connection Diagram

Order Number LF147J, LF347M, LF347BN, LF347N, LF147D/883 or LF147J/883
See NS Package Number D14E, J14A, M14A or N14A
Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>LF147</th>
<th>LF347B/LF347</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>22V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>38V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>19V</td>
</tr>
<tr>
<td>Output Short Circuit Duration (Note 2)</td>
<td>Continuous</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>900 mW</td>
</tr>
<tr>
<td>TJ max</td>
<td>150°C</td>
</tr>
<tr>
<td>IA</td>
<td>150mA</td>
</tr>
<tr>
<td>Cavity DIP (D) Package</td>
<td>80°C/W</td>
</tr>
<tr>
<td>Ceramic DIP (J) Package</td>
<td>70°C/W</td>
</tr>
<tr>
<td>Plastic DIP (N) Package</td>
<td>75°C/W</td>
</tr>
<tr>
<td>Surface Mount Narrow (M)</td>
<td>100°C/W</td>
</tr>
<tr>
<td>Surface Mount Wide (WM)</td>
<td>85°C/W</td>
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DC Electrical Characteristics

(Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LF147</th>
<th>LF347B</th>
<th>LF347</th>
</tr>
</thead>
<tbody>
<tr>
<td>VO</td>
<td>Input Offset Voltage</td>
<td>V(S) = 15V, TA = 25°C Over Temperature</td>
<td>1 5 8</td>
<td>3 5 7</td>
<td>5 10 13 mV</td>
</tr>
<tr>
<td>DVOSS/DT</td>
<td>Average TC of Input Offset Voltage</td>
<td>RS = 10 kX</td>
<td>10</td>
<td>10</td>
<td>10 mV/°C</td>
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<tr>
<td>IO</td>
<td>Input Offset Current</td>
<td>TJ = 25°C, (Notes 5, 6) Over Temperature</td>
<td>25 100 25</td>
<td>25 100 4</td>
<td>25 100 4 pA</td>
</tr>
<tr>
<td>IB</td>
<td>Input Bias Current</td>
<td>TJ = 25°C, (Notes 5, 6) Over Temperature</td>
<td>50 200 50</td>
<td>50 200 8</td>
<td>50 200 8 pA</td>
</tr>
<tr>
<td>RIN</td>
<td>Input Resistance</td>
<td>TJ = 25°C</td>
<td>1012</td>
<td>1012</td>
<td>1012 X</td>
</tr>
<tr>
<td>A VOL</td>
<td>Large Signal Voltage Gain</td>
<td>V(S) = ±15V, TA = 25°C Over Temperature</td>
<td>50 100</td>
<td>50 100</td>
<td>25 100 V/mV</td>
</tr>
<tr>
<td>VO</td>
<td>Output Voltage Swing</td>
<td>V(S) = ±15V, RL = 10 kΩ</td>
<td>±12 ±13.5</td>
<td>±12 ±13.5</td>
<td>±12 ±13.5 V</td>
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<tr>
<td>VCM</td>
<td>Input Common-Mode Voltage Range</td>
<td>V(S) = ±15V</td>
<td>±11 -12</td>
<td>±11 -12</td>
<td>±11 -12 V</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>RS ≤ 10 kΩ</td>
<td>80 100</td>
<td>80 100</td>
<td>70 100 dB</td>
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<tr>
<td>PSRR</td>
<td>Supply Voltage Rejection Ratio (Note 7)</td>
<td>80 100</td>
<td>80 100</td>
<td>70 100 dB</td>
<td></td>
</tr>
<tr>
<td>IS</td>
<td>Supply Current</td>
<td></td>
<td>7.2 11</td>
<td>7.2 11</td>
<td>7.2 11 mA</td>
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## AC Electrical Characteristics (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LF147 Min</th>
<th>LF147 Typ</th>
<th>LF147 Max</th>
<th>LF347B Min</th>
<th>LF347B Typ</th>
<th>LF347B Max</th>
<th>LF347 Min</th>
<th>LF347 Typ</th>
<th>LF347 Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Amplifier to Amplifier Coupling</td>
<td>$T_A = 25^\circ C$, $f = 1$ Hz – 20 kHz (Input Referred)</td>
<td>$-120$</td>
<td>$-120$</td>
<td>$-120$</td>
<td>$-120$</td>
<td>$-120$</td>
<td>$-120$</td>
<td>$-120$</td>
<td>$-120$</td>
<td>$-120$</td>
<td>dB</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>$V_S = \pm 15 V, T_A = 25^\circ C$</td>
<td>8</td>
<td>13</td>
<td>8</td>
<td>13</td>
<td>8</td>
<td>13</td>
<td>V/(\mu)s</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-Bandwidth Product</td>
<td>$V_S = \pm 15 V, T_A = 25^\circ C$</td>
<td>2.2</td>
<td>4</td>
<td>2.2</td>
<td>4</td>
<td>2.2</td>
<td>4</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$e_{in}$</td>
<td>Equivalent Input Noise Voltage</td>
<td>$T_A = 25^\circ C$, $R_S = 100\Omega$, $f = 1\text{kHz}$</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>nV/(\sqrt{Hz})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{in}$</td>
<td>Equivalent Input Noise Current</td>
<td>$T_J = 25^\circ C$, $f = 1\text{kHz}$</td>
<td>0.01</td>
<td>0.01</td>
<td>0.01</td>
<td>0.01</td>
<td>pA/(\sqrt{Hz})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 2:** Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

**Note 3:** For operating at elevated temperature, these devices must be derated based on a thermal resistance of $\frac{\Delta T}{\Delta P}$.

**Note 4:** The LF147 is available in the military temperature range $-55^\circ C$ to $125^\circ C$, while the LF347B and the LF347 are available in the commercial temperature range $0^\circ C$ to $70^\circ C$. Junction temperature can rise to $T_J\text{max} = 150^\circ C$.

**Note 5:** Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20 V$ for the LF147 and for $V_S = \pm 15 V$ for the LF347B.

**Note 6:** The input bias currents are junction leakage currents which approximately double for every 10$^\circ C$ increase in the junction temperature, $T_J$. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation: $P_D = T_J = T_{JA} + P_D$ where $P_D$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

**Note 7:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 5 V$ to $\pm 15 V$ for the LF347B and $V_S = \pm 20 V$ to $\pm 5 V$ for the LF147.

**Note 8:** Refer to RETS147X for LF147D and LF147J military specifications.

**Note 9:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

**Note 10:** Human body model, 1.5 k\(\Omega\) in series with 100 pF.
Typical Performance Characteristics

- Input Bias Current
- Supply Current
- Positive Common-Mode Input Voltage Limit
- Negative Common-Mode Input Voltage Limit
- Positive Current Limit
- Negative Current Limit
- Output Voltage Swing
- Gain Bandwidth
- Bode Plot
- Slew Rate
Typical Performance Characteristics (Continued)

- Distortion vs Frequency
- Undistorted Output Voltage Swing
- Open Loop Frequency Response
- Common-Mode Rejection Ratio
- Power Supply Rejection Ratio
- Equivalent Input Noise Voltage
- Open Loop Voltage Gain
- Output Impedance
- Inverter Settling Time
Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier...
Application Hints (Continued)

output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic
**Typical Applications**

**Digitally Selectable Precision Attenuator**

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>$V_D$</th>
<th>Attenuation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0 dB</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>-1 dB</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
<td>-2 dB</td>
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<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>-3 dB</td>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>-4 dB</td>
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<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>5</td>
<td>-5 dB</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>6</td>
<td>-6 dB</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>7</td>
<td>-7 dB</td>
</tr>
</tbody>
</table>

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

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**Long Time Integrator with Reset, Hold and Starting Threshold Adjustment**

\[ V_{OUT} = \int_{V_{TH}}^{V_{IN}} \left( V_{IN} - V_{TH} \right) dt \]

- $V_{OUT}$ starts from zero
- $V_{OUT}$ starts when $V_{IN} = V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero
Universal State Variable Filter

For circuit shown:

- $f_0 = 3$ kHz, $f_{NOTCH} = 9.5$ kHz
- $Q = 3.4$

Passband gain:
- Highpass—0.1
- Bandpass—1
- Lowpass—1
- Notch—10

$\#f_0 \times Q \leq 200$ kHz

$\#10V$ peak sinusoidal output swing without slew limiting to 200 kHz

$\#$See LM148 data sheet for design equations
Physical Dimensions inches (millimeters)

Hermetic Dual-In-Line Package (D)
Order Number LF147D/883
NS Package Number D14E
Physical Dimensions inches (millimeters) (Continued)

Ceramic Dual-In-Line Package (J)
Order Number LF147J or LF147J/883
NS Package Number J14A

S.O. Package (M)
Order Number LF347M
NS Package Number M14A
**Physical Dimensions** inches (millimeters) (Continued)

Molded Dual-In-Line Package (N)
Order Number LF347BN or LF347N
NS Package Number N14A

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