DATA SHEET

For a complete data sheet, please also download:

• The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
• The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
• The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT153
Dual 4-input multiplexer

Product specification
File under Integrated Circuits, IC06

December 1990
Dual 4-input multiplexer

74HC/HCT153

FEATURES
- Non-inverting output
- Separate enable for each output
- Common select inputs
- See ‘253” for 3-state version
- Permits multiplexing from n lines to 1 line
- Enable line provided for cascading (n lines to 1 line)
- Output capability: standard
- I<sub>CC</sub> category: MSI

GENERAL DESCRIPTION
The 74HC/HCT153 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT153 have two identical 4-input multiplexers which select two bits of data from up to four sources selected by common data select inputs (S<sub>0</sub>, S<sub>1</sub>). The two 4-input multiplexer circuits have individual active LOW output enable inputs (1E, 2E) which can be used to strobe the outputs independently. The outputs (1Y, 2Y) are forced LOW when the corresponding output enable inputs are HIGH.

The “153” is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S<sub>0</sub> and S<sub>1</sub>.

The logic equations for the outputs are:

1Y = 1E. (1I<sub>0</sub>.S<sub>1</sub>.S<sub>0</sub> + 1I<sub>1</sub>.S<sub>1</sub>.S<sub>0</sub> + 1I<sub>2</sub>.S<sub>1</sub>.S<sub>0</sub> + 1I<sub>3</sub>.S<sub>1</sub>.S<sub>0</sub>)

2Y = 2E. (2I<sub>0</sub>.S<sub>1</sub>.S<sub>0</sub> + 2I<sub>1</sub>.S<sub>1</sub>.S<sub>0</sub> + 2I<sub>2</sub>.S<sub>1</sub>.S<sub>0</sub> + 2I<sub>3</sub>.S<sub>1</sub>.S<sub>0</sub>)

The “153” can be used to move data to a common output bus from a group of registers. The state of the select inputs would determine the particular register from which the data came. An alternative application is a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

The “153” is similar to the “253” but has standard outputs.

QUICK REFERENCE DATA
GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>l</sub> = 6 ns

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>TYPICAL</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>HC</td>
<td>HCT</td>
</tr>
<tr>
<td>t&lt;sub&gt;PHL&lt;/sub&gt;/t&lt;sub&gt;PLH&lt;/sub&gt;</td>
<td>propagation delay</td>
<td>CL = 15 pF; V&lt;sub&gt;CC&lt;/sub&gt; = 5 V</td>
<td>14</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1I&lt;sub&gt;n&lt;/sub&gt;, 2I&lt;sub&gt;n&lt;/sub&gt; to nY</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>S&lt;sub&gt;n&lt;/sub&gt; to nY</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>nE to nY</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;i&lt;/sub&gt;</td>
<td>input capacitance</td>
<td>3.5</td>
<td>3.5</td>
<td>pF</td>
</tr>
<tr>
<td>C&lt;sub&gt;PD&lt;/sub&gt;</td>
<td>power dissipation capacitance per multiplexer</td>
<td>notes 1 and 2</td>
<td>30</td>
<td>30</td>
</tr>
</tbody>
</table>

Notes
1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in µW):

   \[ P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \]

   where:
   - f<sub>i</sub> = input frequency in MHz
   - f<sub>o</sub> = output frequency in MHz
   - C<sub>L</sub> = output load capacitance in pF
   - V<sub>CC</sub> = supply voltage in V
   - \( \sum (C_L \times V_{CC}^2 \times f_o) \) = sum of outputs
2. For HC the condition is V<sub>i</sub> = GND to V<sub>CC</sub>
   For HCT the condition is V<sub>i</sub> = GND to V<sub>CC</sub> − 1.5 V

ORDERING INFORMATION
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

December 1990 2
## Dual 4-input multiplexer

### PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>SYMBOL</th>
<th>NAME AND FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 15</td>
<td>1E, 2E</td>
<td>output enable inputs (active LOW)</td>
</tr>
<tr>
<td>14, 2</td>
<td>S0, S1</td>
<td>common data select inputs</td>
</tr>
<tr>
<td>6, 5, 4, 3</td>
<td>1I0 to 1I3</td>
<td>data inputs from source 1</td>
</tr>
<tr>
<td>7</td>
<td>1Y</td>
<td>multiplexer output from source 1</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>9</td>
<td>2Y</td>
<td>multiplexer output from source 2</td>
</tr>
<tr>
<td>10, 11, 12, 13</td>
<td>2I0 to 2I3</td>
<td>data inputs from source 2</td>
</tr>
<tr>
<td>16</td>
<td>VCC</td>
<td>positive supply voltage</td>
</tr>
</tbody>
</table>

![Fig.1 Pin configuration.](image1)

![Fig.2 Logic symbol.](image2)

![Fig.3 IEC logic symbol.](image3)

![Fig.4 Functional diagram.](image4)
Dual 4-input multiplexer

**FUNCTION TABLE**

<table>
<thead>
<tr>
<th>SELECT INPUTS</th>
<th>DATA INPUTS</th>
<th>OUTPUT ENABLE</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>S1</td>
<td>nI0</td>
<td>nI1</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>X</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>X</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**Note**

1. H = HIGH voltage level
2. L = LOW voltage level
3. X = don’t care

**Fig.5** Logic diagram.
Dual 4-input multiplexer 74HC/HCT153

DC CHARACTERISTICS FOR 74HC
For the DC characteristics see “74HC/HCT/HCU/HCMOS Logic Family Specifications”.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC
GND = 0 V; t_{r} = t_{f} = 6 ns; C_{L} = 50 pF

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>T_{amb} (°C)</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>+25</td>
<td>−40 to+85</td>
</tr>
<tr>
<td></td>
<td></td>
<td>min.</td>
<td>typ.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>47</td>
<td>145</td>
</tr>
<tr>
<td></td>
<td></td>
<td>17</td>
<td>29</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50</td>
<td>150</td>
</tr>
<tr>
<td></td>
<td></td>
<td>18</td>
<td>30</td>
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<td>14</td>
<td>26</td>
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<td></td>
<td></td>
<td>33</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>19</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6</td>
<td>13</td>
</tr>
</tbody>
</table>
Dual 4-input multiplexer 74HC/HCT153

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see “74HC/HCT/HCU/HCMOS Logic Family Specifications”.

Output capability: standard

\( I_{CC} \) category: MSI

**Note to HCT types**

The value of additional quiescent supply current (\( \Delta I_{CC} \)) for a unit load of 1 is given in the family specifications. To determine \( \Delta I_{CC} \) per input, multiply this value by the unit load coefficient shown in the table below.

<table>
<thead>
<tr>
<th>INPUT</th>
<th>UNIT LOAD COEFFICIENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_1 ), ( 2I_e )</td>
<td>0.45</td>
</tr>
<tr>
<td>( nE )</td>
<td>0.60</td>
</tr>
<tr>
<td>( S_n )</td>
<td>1.35</td>
</tr>
</tbody>
</table>

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; \( t_r = t_f = 6 \) ns; \( C_L = 50 \) pF

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>( T_{amb} (\degree C) )</th>
<th>( V_{cc} ) (V)</th>
<th>WAVEFORMS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>74HCT</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>+25</td>
<td>-40 to +85</td>
<td>-40 to +125</td>
</tr>
<tr>
<td></td>
<td></td>
<td>min.</td>
<td>typ.</td>
<td>max.</td>
</tr>
<tr>
<td>( t_{PHL} )</td>
<td>propagation delay ( 1I_1 ) to ( nY ); ( 2I_1 ) to ( nY )</td>
<td>19</td>
<td>34</td>
<td>43</td>
</tr>
<tr>
<td>( t_{PLH} )</td>
<td>propagation delay ( 1I_1 ) to ( nY ); ( 2I_1 ) to ( nY )</td>
<td>13</td>
<td>24</td>
<td>30</td>
</tr>
<tr>
<td>( t_{PHL}/t_{PLH} )</td>
<td>propagation delay ( S_n ) to ( nY )</td>
<td>20</td>
<td>34</td>
<td>43</td>
</tr>
<tr>
<td>( t_{PHL}/t_{PLH} )</td>
<td>propagation delay ( nE ) to ( nY )</td>
<td>14</td>
<td>27</td>
<td>34</td>
</tr>
<tr>
<td>( t_{THL}/t_{TLH} )</td>
<td>output transition time</td>
<td>7</td>
<td>15</td>
<td>19</td>
</tr>
</tbody>
</table>
Dual 4-input multiplexer

AC WAVEFORMS

Fig. 6 Waveforms showing the input \( (1I_n, 2I_n) \) to output \( (1Y, 2Y) \) propagation delays and the output transition times.

(1) HC : \( V_M = 50\% \); \( V_I = \text{GND to } V_{CC} \).
HCT: \( V_M = 1.3 \text{ V} \); \( V_I = \text{GND to } 3 \text{ V} \).

Fig. 7 Waveforms showing the select input \( (S_0, S_1) \) and the output enable input \( (E) \) to output \( (1Y, 2Y) \) propagation delays and the output transition times.

(1) HC : \( V_M = 50\% \); \( V_I = \text{GND to } V_{CC} \).
HCT: \( V_M = 1.3 \text{ V} \); \( V_I = \text{GND to } 3 \text{ V} \).

PACKAGE OUTLINES

See “74HC/HCT/HCU/HCMOS Logic Package Outlines”.